APPLICATION NOTE
UnitedSiC_AN0023 – June 2020, Revision 2

3L-ANPC vs. 3L-NPC Inverters

By Jonathan Dodge, P.E.

Abstract

Three-level diode neutral point clamped (3L-NPC) and active neutral point clamped (3L-ANPC) inverters share fundamental features, including an operating voltage limit that is higher than the individual power semiconductor ratings, reduced switching loss, and three-level output voltages. Neutral point voltage balancing algorithms remain unchanged. In the 3L-ANPC, two FETs replace two diodes in each leg, and therefore 3L-ANPC is higher cost. Depending on modulation, the additional 3L-ANPC switch states can be used to reduce power loss, double the output frequency, and/or affect switch utilization. Midpoints between series FETs are periodically clamped, eliminating the need for balancing resistors. Additional destructive switch states must be avoided. Operation of each inverter type is briefly explained, followed by a review of some 3L-ANPC modulation strategies, and finally by steady state power loss calculations. These calculations are very useful for comparing 3L-NPC and 3L-ANPC topologies and modulation strategies, and for selecting the number and type of power semiconductors.

Jonathan Dodge is a Senior Applications Engineer at United Silicon Carbide. Experience includes design of analog, digital, and power electronics; working with power levels ranging from 1.5 to 500 kW in renewable energy and other applications.

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1 Introduction

UnitedSiC cascode FETs are a good choice for hard-switched inverters due to the low on-resistance, low reverse recovery charge, and flexible gate drive.

Common features of 3L-NPC and 3L-ANPC include the split DC link and freewheeling paths yielding three output potentials at any power factor in each leg [1-3]. Each AC output connects to DC+, DC- and the neutral point N, which is the center point of the DC link. Clamping of the output to the neutral point in 3L-NPC requires turning on both inner FETs, Q2 and Q3 shown in the single leg diagram Figure 1 (a). Clamping in 3L-ANPC is through two selectable paths, one through a common-drain pair Q2 and Q5, another through a common-source pair Q3 and Q6, or through both paths simultaneously.

The FETs mentioned here are UnitedSiC cascodes, which have automatic reverse conduction similar to a MOSFET. The reverse recovery charge is low, allowing hard commutation without a separate diode. However, to extend power loss equations to devices with anti-parallel diodes (particularly IGBTs), it is to be understood that Q1 refers to a forward-conducting FET Q1 and an implied (intrinsic) diode D1, and so on, even though the intrinsic diode feature is not labelled separately in the circuit diagrams.

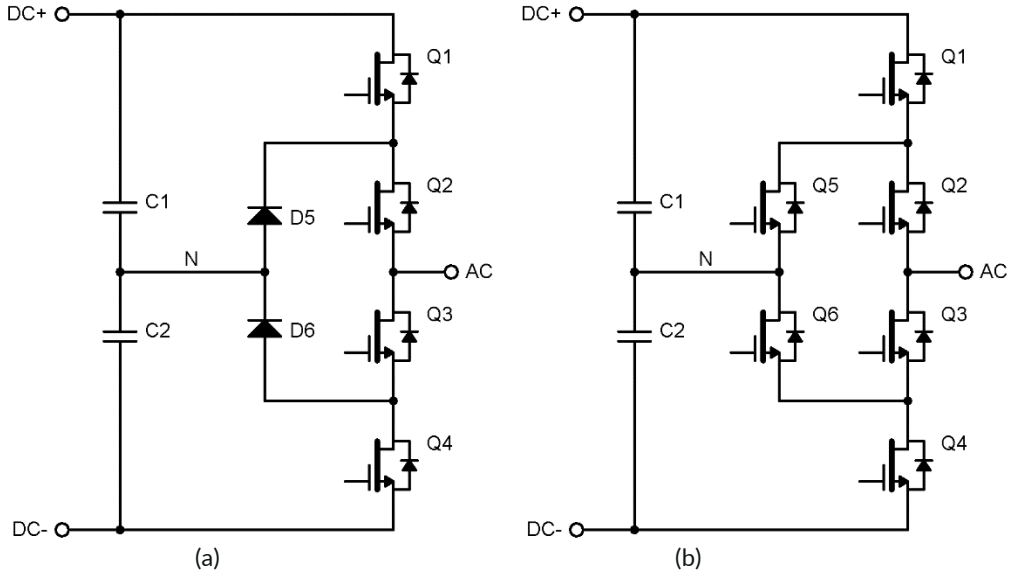


Figure 1 (a) 3L-NPC phase leg, and (b) 3L-ANPC phase leg

The 3L-ANPC was introduced in [6], and much focus since has been on balancing power loss between FETs to improve switch utilization [6, 7, 11-14]. The modulation strategies PWM1 or PWM2 presented in [9, 10] keep the most power loss in the outer FETs Q1 and Q4, or in the inner FETs Q2 and Q3 respectively. These two can be combined based on power loss or temperature calculations [6, 7, 11-14], however this will not be discussed in this application note. Modulation strategy PWM3 leads to a natural doubling of the apparent frequency, which of course simplifies the line filter design, an advantage important for applications requiring reduced size and weight, but at the expense of higher switching loss. Another modulation strategy presented in [5] turns on all but the outer FETs for a single neutral state that reduces conduction loss overall and switching stress on the clamp FETs. For sake of clarity, we will call this modulation strategy PWM4. PWM1-4 implicitly apply to the 3L-ANPC topology.

Section 2 details safe, hazardous and destructive switch states. Each PWM strategy is briefly outlined in Section 3, along with controller requirements. Section 4 explains the calculation method for conduction and switching power loss estimates for each modulation strategy. In section 5, these formulas are applied to example inverter designs utilizing low $R_{DS(on)}$ FETs from UnitedSiC, facilitating comparisons and tradeoff analysis. The results are summarized in Section 6. Power loss equations are listed in the appendix.

2 Safety First

In [1, 2] the safe, hazardous, and destructive 3L-NPC states are thoroughly analyzed. The 3L-ANPC phase leg adds 48 possible switch states to the 16 in 3L-NPC. With Q5 and Q6 off, the same hazardous and destructive switch states apply to 3L-ANPC as to 3L-NPC. With Q5 and/or Q6 on, a few states are no longer hazardous due to voltage clamping. Table 1 below lists all 3L-ANPC disallowed switch states, with 1 or 0 representing the corresponding FET being on or off respectively, and 'X' represents a "don't care" whether the FET is on or off.

With six active switches per leg, there are many options for 3L-ANPC modulation, but they must all avoid the switch states listed in Table 1, including transitions between switch states.

State \ FETs	Q1	Q2	Q3	Q4	Q5	Q6
Hazardous	1	0	0	0	0	0
	1	0	1	0	0	0
	0	0	0	1	0	0
	0	1	0	1	0	0
	1	0	0	1	0	0
Destructive	1	1	1	X	X	X
	1	1	X	1	X	X
	1	X	1	1	X	X
	X	1	1	1	X	X
	1	X	X	X	1	X
	X	X	X	1	X	1

Table 1 3L-ANPC disallowed switch states

The first two rows of hazardous states in Table 1 can be made safe with Q6 already on, which clamps the output to the neutral point for positive current in Figure 1(b) (current leaving the AC terminal). These states are safe with negative current but having Q6 on maintains voltage balance between Q3 and Q4. Similarly, the third and fourth hazardous states in Table 1 become safe with Q5 on. Additional destructive states apply to 3L-ANPC, namely whenever Q1 and Q5 or Q4 and Q6 are on simultaneously, in the bottom two rows of Table 1.

3 Modulation Strategies

The modulation of a multilevel converter is facilitated by the concept of commutation cells, where FETs are grouped based on the modulation strategy. FETs in a commutation cell are often complementary switching pairs; they have opposite switch states but can sometimes be both off, such as during deadtime. With sinusoidal PWM (SPWM) or most space vector modulation (SVM) strategies, during a half line cycle, at least one cell remains static while the others switch at the switching frequency.

3.1 3L-NPC

The switching sequence for 3L-NPC is relatively straightforward: Q1 and Q3 as well as Q2 and Q4 form complementary commutation cells. Cell 1 and cell 2 alternate between line and switching frequency during negative and positive half line cycles respectively.

All safe 3L-NPC switch states are used. This is not the case for 3L-ANPC.

		Cell 1		Cell 2	
V_{xN}	State \ FETs	Q1	Q3	Q2	Q4
V_{DC} / 2	P	1	0	1	0
0	O	0	1	1	0
-V_{DC} / 2	N	0	1	0	1

Table 2 Switch states for an 3L-NPC phase leg

Table 2 shows that the 3L-NPC O state is reached by switching on Q2 and Q3, with the outer FETs Q1 and Q4 already switched off of course. The current path during the O state is determined by the current direction and cannot be selected; forward current flows through D5 and Q2, whereas reverse current flows through Q3 and D6. State transitions are explained in [2], as well as how two PWM channels in a microcontroller can directly control one 3L-NPC phase leg.

3.2 3L-ANPC PWM1

With PWM1 strategy, cell 2 always switches at line frequency, and cells 1 and 3 alternate between line and switching frequency during negative and positive half line cycles respectively.

		Cell 1		Cell 2		Cell 3	
V_{xN}	FETs / State	Q1	Q5	Q2	Q3	Q6	Q4
VDC / 2	P	1	0	1	0	0	0
0	O^+	0	1	1	0	0	0
	O^-	0	0	0	1	1	0
-VDC / 2	N	0	0	0	1	0	1

Table 3 PWM1 switch states for an 3L-ANPC phase leg

PWM1 strategy is advantageous for 3L-ANPC with each commutation cell implemented with a half-bridge module and operating at unity power factor because only short commutation paths are used.

PWM1 strategy is similar to 3L-NPC modulation with synchronous rectification of Q5 and Q6, except current is forced through Q2 and Q5 in the O^+ state during positive half cycle, and through Q3 and Q6 in the O^- state during negative half cycle. In this way, only short commutation paths are used.

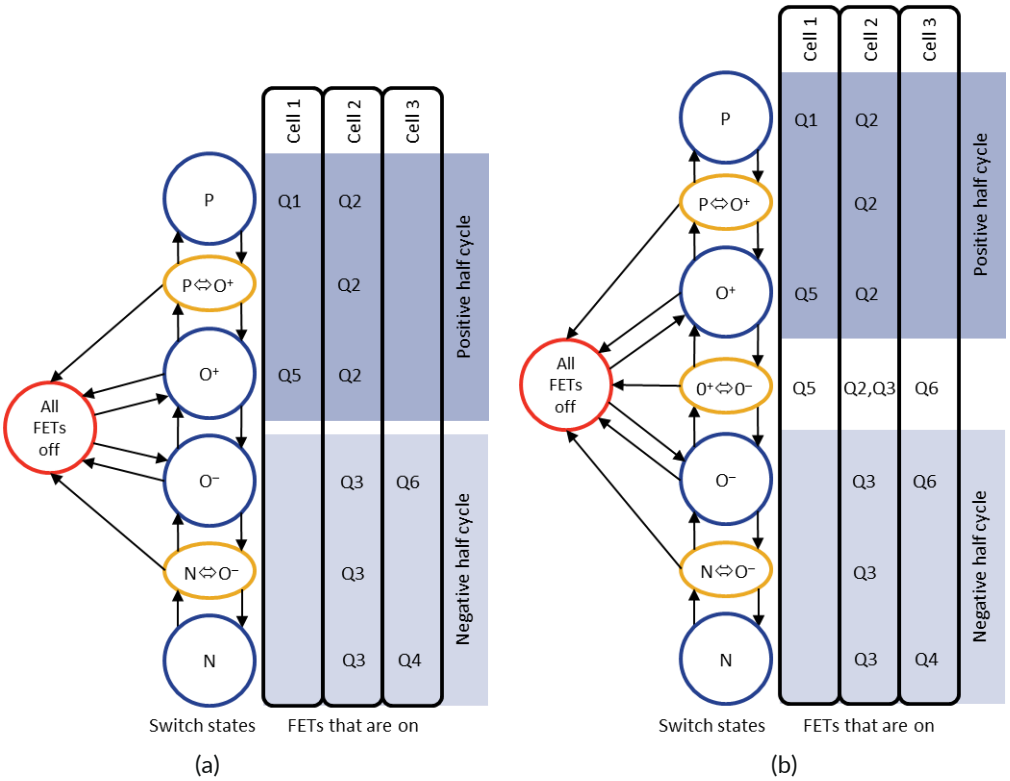


Figure 2 PWM1 state diagram for a 3L-ANPC phase leg; simple (a), and glitch-free (b)

Something not discussed in the literature is the transitions between positive and negative half cycles. Figure 2(a) shows a state transition diagram corresponding to Table 3, but necessary

transition states are added, which represent the switch states during deadtimes. These must be considered to ensure safe operation. Beginning from an OFF state when all FETs are off, the next state can be any except P or N to avoid a race condition between Q1 and Q2 or Q3 and Q4 switching on and possibly causing an overvoltage transient of Q2 or Q3. In Figure 2, the state transitions from OFF to either O^+ or O^-, and back to OFF from one of these states for normal shutdown. Emergency shutdown can be from any state except P and N. This state transition diagram is for example only because other implementations can be safe.

There is a potential problem with Figure 2(a) because multiple cells switch during the transition between positive and negative half cycles. This poses no risk of damage to the FETs; Q2, Q3, Q5, and Q6 can switch safely in any sequence, or even remain on. However, there can be a glitch in the output voltage, depending on the current polarity (negative during positive half wave voltage, positive during negative half wave). If such glitches are unlikely or are acceptable, then there is no need to implement a deadtime between O^+ and O^- transitions, as shown in Figure 2(a). To avoid any output voltage glitches regardless of power factor, then a transition state must be added as shown in Figure 2(b). In this case, FETs are switched on instead of off, allowing current to flow freely through either the upper or lower clamp path. This allows seamless NP balancing such as nearest three virtual space vectors (NTVSV) [4].

Three PWM channels in a microcontroller can directly control one phase leg, but to implement the transition state in Figure 2(b) would require cycle-by-cycle PWM register updates, at least near the voltage zero crossing, which is commonly the case with SVM anyway. Alternatively, programmable logic can be added to reduce the microcontroller resource and computation load.

3.3 3L-ANPC PWM2

With PWM2 strategy, cell 2 always switches at the switching frequency, and cells 1 and 3 always at line frequency. This causes most switching stress to be in cell 2 and practically none in cells 1 and 3, regardless of power factor.

		Cell 1		Cell 2		Cell 3	
V_{xN}	FETs / State	Q1	Q5	Q2	Q3	Q6	Q4
VDC / 2	P	1	0	1	0	1	0
0	O^+	1	0	0	1	1	0
	O^-	0	1	1	0	0	1
-VDC / 2	N	0	1	0	1	0	1

Table 4 PWM2 switch states for a 3L-ANPC phase leg

The idea behind PWM2 is to save cost in 3L-ANPC by using lower performance power semiconductors for all switch positions except Q2 and Q3.

Current is forced through Q3 and Q6 in the O^+ state during positive half cycle, and through Q2 and Q5 in the O^- state during negative half cycle. In this way, only long commutation paths are used, but the switching loss is focused on only two of the six FETs in each phase leg. Q6 is kept on during the P state to balance voltage between Q3 and Q4, which are off. Similarly, Q5 balances the voltage between Q1 and Q2 during the N state.

Figure 3(a) shows a state transition diagram corresponding to Table 4, but necessary transition deadtime states are added. Beginning from an OFF state, the next state can be any except P or N to avoid a race condition between Q1, Q2, and Q6; or between Q3, Q4, and Q5, possibly causing an overvoltage transient of Q2 or Q3. In Figure 3(a), the state transitions from OFF to either O^+ or O^-, and back to OFF from one of these states for normal shutdown. Emergency shutdown can be from any state except P and N.

Because Q1 and Q5 can never be on simultaneously, and neither can Q4 and Q6, a deadtime is needed between states 0^+ and 0^-. It is implied that all FETs switch off during this deadtime, which means the output voltage is indeterminate, and there could be an output voltage glitch, although the FETs are safe. If output voltage glitches must be avoided, then transition deadtime states must be added as shown in Figure 3(b). In states $0^+ \Leftrightarrow 0^-$ DT1 and $0^+ \Leftrightarrow 0^-$ DT3, FETs Q6 and Q3 respectively can be either on or off and so are listed in gray. State $0^+ \Leftrightarrow 0^-$ DT2

is the familiar O state for a 3L-NPC phase leg and so makes a natural choice to exit/enter the OFF state during normal operation. These state transition diagrams are for example only because other implementations can be safe.

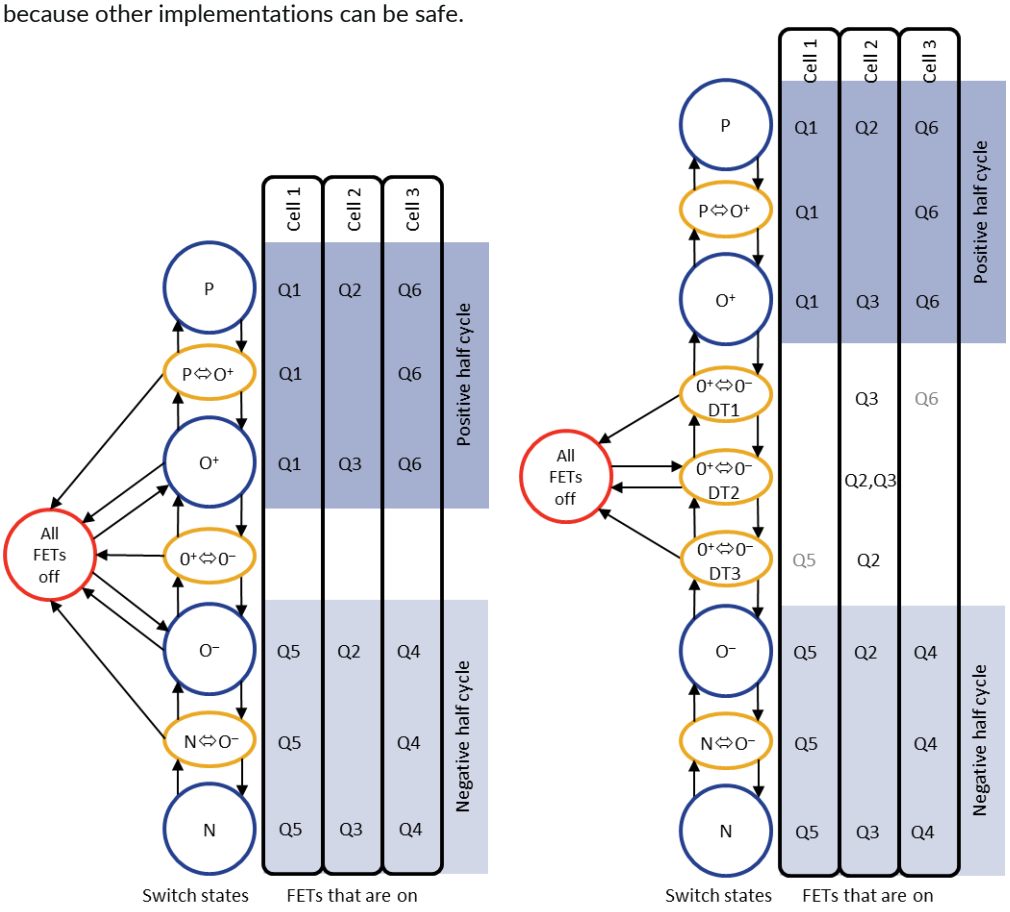


Figure 3 PWM2 state diagram for a 3L-ANPC phase leg; simple (a), and glitch-free (b)

Three PWM channels in a microcontroller with rising and falling deadtime would follow the state transitions of Figure 3(a). To implement the transition state in Figure 2(b) would require cycle-by-cycle PWM register updates near the voltage zero crossing or programmable logic.

3.4 3L-ANPC PWM3

With PWM3 strategy, all cells switch at the switching frequency. Cells 1 and 3 have no switching loss during the negative and positive half cycles respectively, but both have regular switching loss otherwise. More switching events doubles the frequency at the AC terminal.

PWM3 trades higher switching loss for doubling the AC terminal frequency and more uniform switch utilization.

		Cell 1		Cell 2		Cell 3	
V_{xN}	FETs / State	Q1	Q5	Q2	Q3	Q6	Q4
VDC / 2	P	1	0	1	0	1	0
0	O_1^+	0	1	1	0	0	0
	O_2^+	1	0	0	1	1	0
	O_1^-	0	0	0	1	1	0
	O_2^-	0	1	1	0	0	1
-VDC / 2	N	0	1	0	1	0	1

Table 5 PWM3 switch states for a 3L-ANPC phase leg

There are four neutral states. Current is forced through Q2 and Q5 in the O_1^+ state, and through Q3 and Q6 during the O_2^+ state; both states used during positive half cycle. Similarly, states O_1^- and O_2^- force current through Q3 and Q6 or through Q2 and Q5 respectively, all during the negative half cycle. Both short and long commutation paths are used during each switching cycle. In fact, PWM3 is a combination of PWM1 and PWM2 within each switching cycle. As with PWM2, Q5 and Q6 balance the voltage between Q1 and Q2, and Q3 and Q4 during the N and P states.

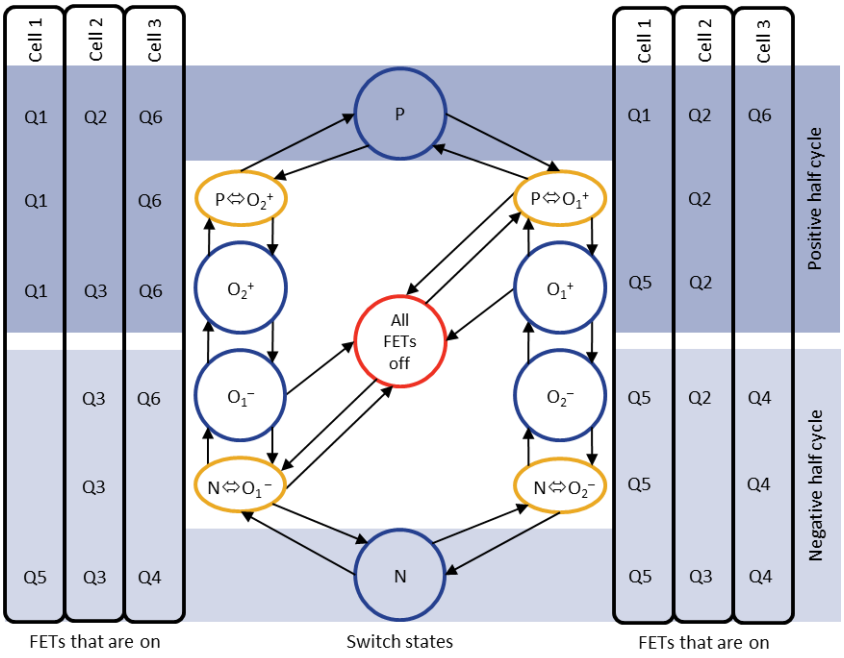


Figure 4 PWM3 state diagram for a 3L-ANPC phase leg

Figure 4 shows a state transition diagram corresponding to Table 5, but necessary transition deadtime states are added as before. FETs that are on are shown on both sides of this state diagram for clarity because states transition from one side through the P or N state to the other side and back during one switching cycle. The state transitions shown in the top right portion of Figure 4 during the positive half cycle are the same as for PWM1, and the top left match PWM2. Similarly, the bottom left and right sides correspond to PWM1 and PWM2 respectively. Transitions between positive and negative voltage half cycles are seamless (no output glitches) and require no added deadtime states.

As with PWM2, the next state from the OFF state can be any except P or N to avoid a race condition between Q1, Q2, and Q6; or Q3, Q4, and Q5 switching on and possibly causing an overvoltage transient of Q2 or Q3. In Figure 4, the state transitions from OFF to either $P⇔O_1^+$ or $N⇔O_1^-$, and back to OFF from one of these states for normal shutdown. Emergency shutdown can be from any state except P and N. Just as before, these state transition diagrams are for example only because other implementations can be safe. In fact, [6, 7] mention switching Q6 on last and off first during transitions between P and O_1^+ states, and similarly Q5 switches on after and off before Q4 between states N and O_1^-. Presumably this prevents a race condition between the two clamp paths, although switching on both paths is safe. In fact, it is the core of what we call here 3L-ANPC PWM4 modulation strategy.

PWM3 can be implemented with three PWM channels in a microcontroller by reconfiguring the PWM registers at each zero-voltage crossing. However, given the alternating switching patterns, use of programmable logic seems to be a natural choice.

3.5 3L-ANPC PWM4

With PWM4 strategy, FETs can be grouped into two commutation cells, with two FETs in each cell switching together. Cell 1 and cell 2 alternate between line and switching frequency during negative and positive half line cycles respectively. A unique feature is a single neutral state.

		Cell 1			Cell 2		
V_{xN}	FETs / State	Q1	Q3	Q5	Q4	Q2	Q6
VDC / 2	P	1	0	0	0	1	1
0	O	0	1	1	0	1	1
-VDC / 2	N	0	1	1	1	0	0

Table 6 PWM4 switch states for a 3L-ANPC phase leg

The simpler PWM4 strategy reduces conduction loss. FETs such as UnitedSiC cascodes with equal forward and reverse on-resistance and no "knee" voltage yield the full benefits of PWM4.

Current can flow in either direction through both clamp paths, which reduces the conduction loss in the corresponding FETs, while the total switching loss remains practically the same as a single clamp path [5]. Using FETs with equal forward and reverse conduction loss, such as UnitedSiC cascodes, the conduction loss is halved in each clamp FET during the neutral state. Efficiency is further improved by using FETs without a forward or reverse "knee voltage", which is especially important at lower current.

Figure 5 shows a state transition diagram corresponding to Table 6 with transition deadtime states added. Beginning from an OFF state, a logical choice for the next state is O. Transition to OFF can be from any state except P or N. Transitions between negative and positive half cycles involve a switching event in only one cell, so there is no chance of output voltage glitches and no need for additional transition states. As with PWM2 and PWM3, Q5 and Q6 balance the voltage between Q1 and Q2, and Q3 and Q4 during the N and P states.

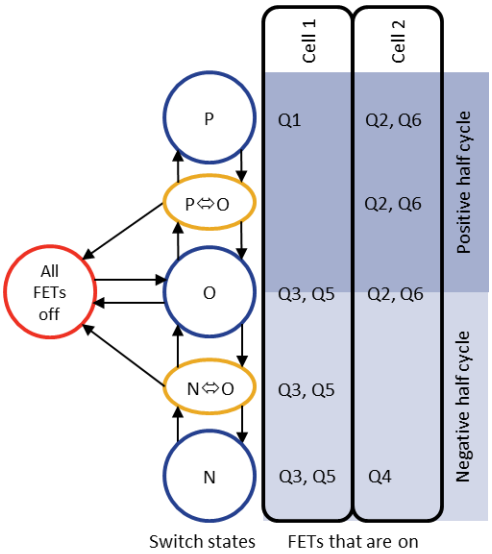


Figure 5 PWM4 state diagram for a 3L-ANPC phase leg

PWM4 is easily implemented with two microcontroller PWM channels per 3L-ANPC phase leg, similar to 3L-NPC, and NTVSV or other neutral point balancing schemes require no extra states.

4 Power Loss Calculation Method

A simplifying assumption facilitates the derivation of closed form solutions for conduction loss calculations, namely that of infinite switching frequency. The implications of this simplification include:

- Effect of current ripple in the line filter is ignored
- Effect of deadtime is ignored
- The ratio of switching to fundamental frequency is considered very large, ignoring the effect of a finite number of pulses within a line half cycle

Furthermore, sine-triangle PWM (SPWM) is used, which greatly simplifies the analysis. However, space-vector modulation (SVM) has fewer switching events per switching cycle in a three-phase inverter, and hence lower switching loss [4, 5]. A correction factor can easily be applied to the switching loss equations to account for this. SPWM is used here for comparison purposes, with the understanding that the power loss would be somewhat lower with SVM.

A word about accuracy is in order. The purpose of loss estimation is to gain a general understanding of circuit performance with various devices and operating conditions. The estimates must be accurate enough to make meaningful comparisons and basic design decisions such as which topology is best for a certain application, which devices to populate in it, and how many devices to parallel, if any. An accuracy of 10 to 20 % suffices for these purposes and is within the capability of these loss calculations, given the simplifying assumptions and differences between datasheet test circuits and conditions and end applications. Higher accuracy requires dynamic simulations or testing with hardware.

4.1 Conduction Loss

A functional simulation is immensely helpful for setting up the power loss equations. Such a simulation as in Figure 6 shows the modulation (control) signal, the electrical angle θ, phase current lagging by the phase angle φ, the forward current through Q1, reverse current through D1 (really the intrinsic diode of Q1 if it is a FET), and the gate control signal for Q1.

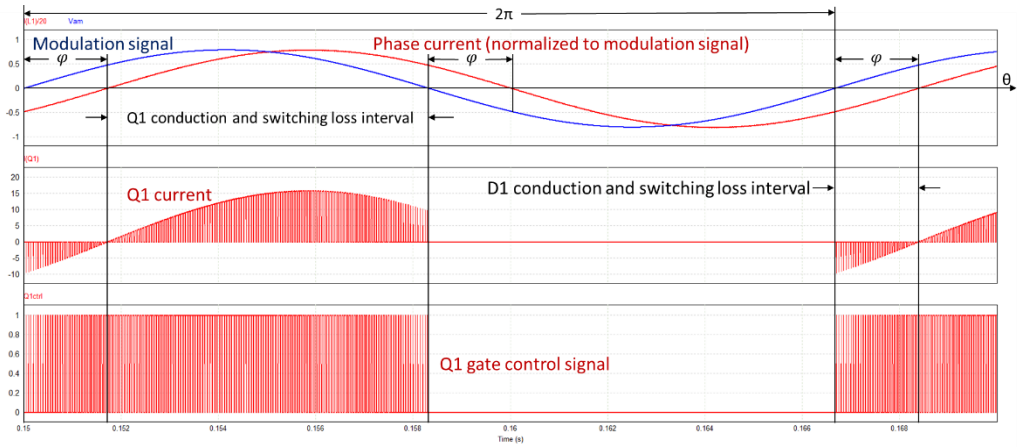


Figure 6 Phase angle, conduction, and switching loss intervals for 3L-ANPC PWM1

One complete AC line cycle spans 2π radians of θ, but Q1 conducts forward (positive) current only during half a line cycle.

$$P_{cQ1} = \frac{1}{2\pi}\sum\left[R_{ds}\left(I_{pk}\sin(\theta-\varphi)\right)^2 + V_0 I_{pk}\sin(\theta-\varphi)\right]\tau(\theta) \quad (1)$$

In equation (1), $\tau(\theta)$ is a switching function with a value of 0 or 1 when the Q1 gate signal is off or on respectively. This is where the infinite switching frequency simplification comes into play. The switching function $\tau(\theta)$ is replaced by a continuous modulation function that has a range of

0 to 1. This modulation function is the equation of the modulation signal, as in equation (2) where m is the modulation index and I_{pk} is the peak current in a single FET since we are solving for the per FET power loss. R_{ds} is the FET $R_{DS(on)}$, and V_0 is the knee voltage of the FET, which is always zero for UnitedSiC FETs, but including it allows the equations to be applied to bipolar type devices such as IGBTs with output characteristic modelled as a straight line with an offset.

$$P_{cQ1} = \frac{1}{2\pi}\int_{\varphi}^{\pi}\left[R_{ds}\left(I_{pk}\sin(\theta-\varphi)\right)^2 + V_0 I_{pk}\sin(\theta-\varphi)\right] m\cdot\sin(\theta)\,d\theta \quad (2)$$

The limits of integration correspond to the modulation function, and the phase angle φ accounts for reactive power. The equation could alternatively be written as follows with the same result.

$$P_{cQ1} = \frac{1}{2\pi}\int_{0}^{\pi-\varphi}\left[R_{ds}\left(I_{pk}\sin(\theta)\right)^2 + V_0 I_{pk}\sin(\theta)\right] m\cdot\sin(\theta+\varphi)\,d\theta \quad (3)$$

The result of evaluating this integral is:

$$P_{cQ1} = \frac{m}{12\pi}\cdot\left[2I_{pk}^2 R_{DS}(1+\cos(\varphi))^2 + 3I_{pk}V_0[(\pi-\varphi)\cos(\varphi)+\sin(\varphi)]\right] \quad (4)$$

Referring to Figure 1, due to symmetry, the power loss in Q4 equals that in Q1, and likewise the power losses in Q3 and Q6 (or D6) equal those in Q2 and Q5 (or D5) respectively. For brevity therefore, power loss equations refer only to Q1, Q2, and Q5 (or D5).

The equation to calculate the reverse conduction loss in D1 (Q1 intrinsic diode) is:

$$P_{cD1} = \frac{1}{2\pi}\int_{0}^{\varphi}\left[R_{ds}\left(-I_{pk}\sin(\theta-\varphi)\right)^2 - V_0 I_{pk}\sin(\theta-\varphi)\right] m\sin(\theta)\,d\theta \quad (5)$$

In equation (5), the current was negated because during the D1 conduction loss interval, the phase current is negative, but a negative current multiplied by V_0, the knee voltage of D1, would result in a negative power loss, which is arguably impossible. With synchronous rectification, which is always used in inverters, and ignoring deadtime, V_0 is zero for UnitedSiC FETs as before. The result of evaluating equation (5) is:

$$P_{cD1} = \frac{m}{12\pi}\cdot\left[2I_{pk}^2 R_{DS}(1-\cos(\varphi))^2 + 3I_{pk}V_0[-\varphi\cos(\varphi)+\sin(\varphi)]\right] \quad (6)$$

In a similar manner, conduction loss equations were derived for each switch position of 3L-NPC and 3L-ANPC and for each modulation strategy. The results are listed in the appendix.

4.2 Switching Loss

Switching loss can be modelled as a second-order polynomial, with data taken from datasheet graphs, and adjusted for temperature. For example, the turn-on switching energy versus drain current I_d is modelled as in equation (7) below where a_{sw}, b_{sw}, and c_{sw} are polynomial coefficients.

$$E_{on} = a_{sw}\cdot I_d^2 + b_{sw}\cdot I_d + c_{sw} \quad (7)$$

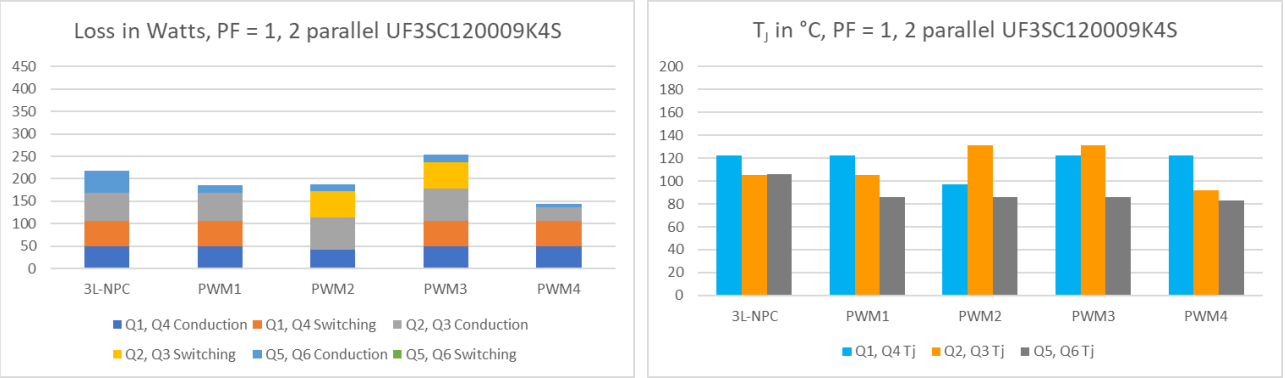
The coefficients are used in an integral to calculate switching loss, similar to conduction loss.

$$P_{swQ1} = \left[\frac{1}{2\pi}\int_{\varphi}^{\pi}\left[a_{sw}\left(I_{pk}\sin(\theta-\varphi)\right)^2 + b_{sw}I_{pk}\sin(\theta-\varphi) + c_{sw}\right]d\theta\right]\frac{V_{DC}/_2}{V_{ref}}f_{sw} \quad (8)$$

It is reasonable to assume that the switching loss scales with the total DC link voltage, which is V_{DC} in equation (2). Note that only half the DC link voltage is switched in a three-level inverter, so V_{DC} is divided by 2. The voltage used to characterize the switching energies in the datasheet is V_{ref}, and f_{sw} is the switching frequency. Switching loss equations are listed in the appendix.

5 Calculation Example

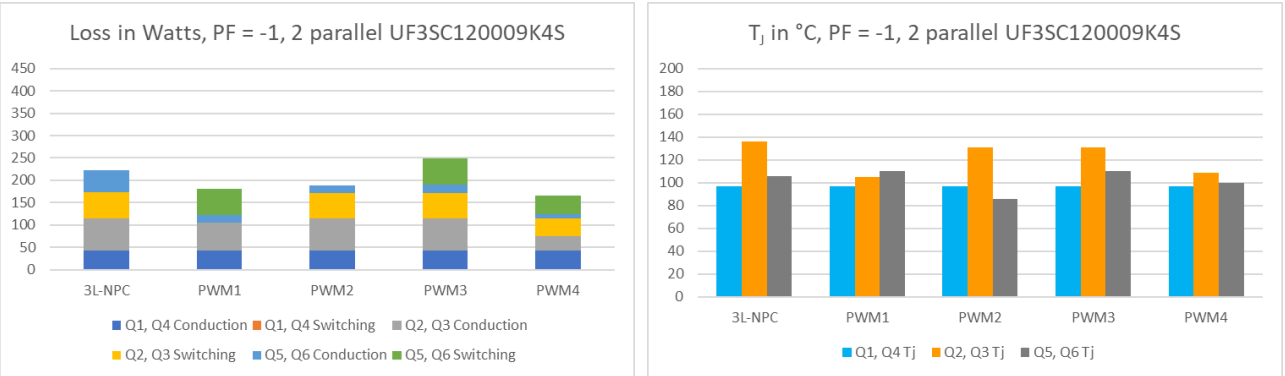
Imagine a 150 kVA three-phase inverter that can be used at +/-1 power factor (inverter or rectifier mode). The total DC voltage can reach 1500 V, but calculations can be done at the nominal value of 1160 V. The switching frequency is a modest 25 kHz. The AC line-to-line voltage is 600 V rms. Will discrete parts work, and if so, which parts? Which topology and PWM scheme would be best? Some power loss calculations can help to answer these questions. In the following figures, the heat sink temperature is assumed steady at 80 °C, and each FET has a phase change isolator pad with 0.6 °C/W thermal resistance. Two parallel UJ3D1250K2 SiC Schottky diodes occupy switch positions D5 and D6 in the 3L-NPC inverter. Also, the $R_{DS(on)}$ per FET is automatically adjusted based on the junction temperature. This is possible because there is an equation for $R_{DS(on)}$ versus temperature (second-order polynomial curve fit) and an equation for temperature rise versus power loss, for which the switching loss component is independent of temperature. With these two equations, both $R_{DS(on)}$ and junction temperature can be solved for.



(a) (b)

Figure 7 Inverter mode: (a) power loss in two UF3SC120009K4S per switch position, and (b) junction temperatures

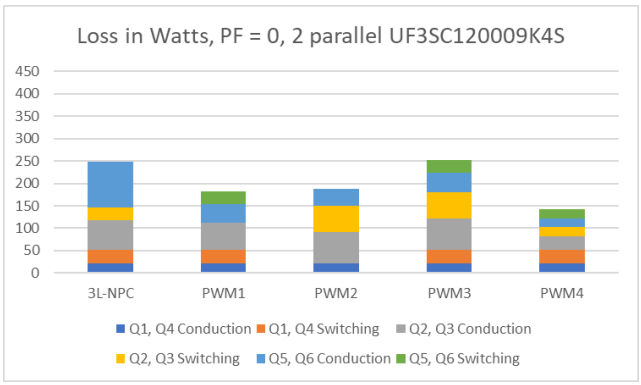
Figure 7(a) shows the combined power loss of two parallel UF3SC120009K4S FETs per switch position (except in the 3L-NPC which uses two parallel UJ3D1250K2 for D5 and D6). The benefit of synchronous rectification of Q5 and Q6 is evident in 3L-NPC and PWM1. PWM4 clearly has the lowest total losses. The FETs in Q5 and Q6 positions are lightly loaded, and those in Q2 and Q3 are modestly loaded, as seen in the PWM4 temperatures in Figure 7(b).



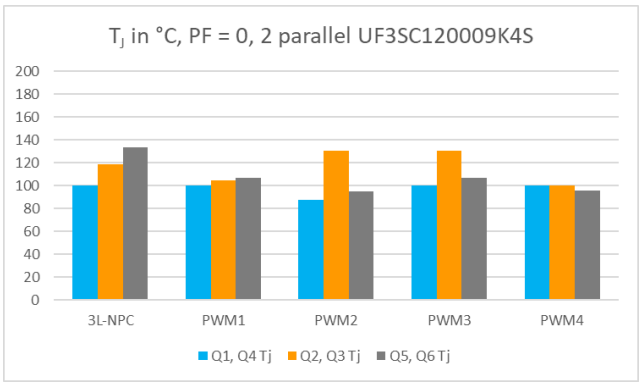
(a) (b)

Figure 8 Rectifier mode: (a) power loss in two UF3SC120009K4S per switch position, and (b) junction temperatures

In Figure 8(a), PWM4 again has the lowest total loss, so it would also be a good choice in a rectifier application, although PWM1 and PWM2 are closer behind.



(a)

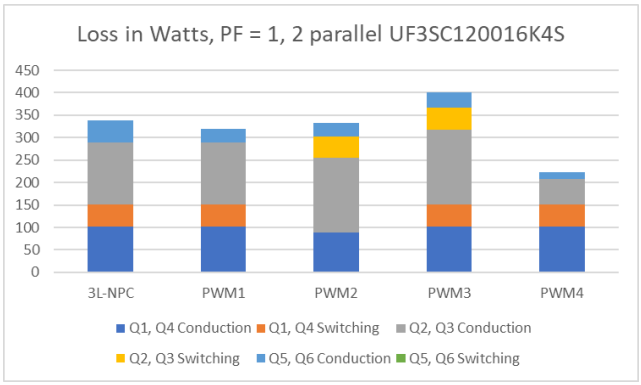


(b)

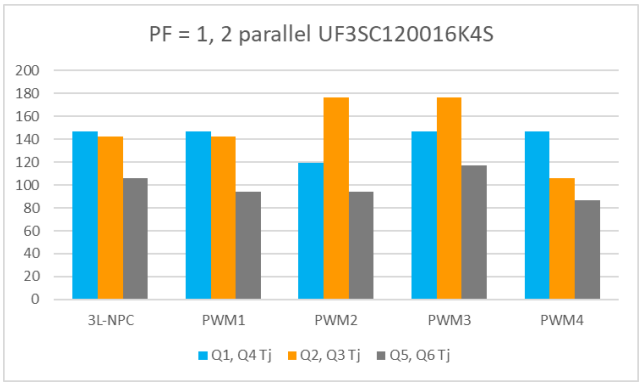
Figure 9 Reactive mode: (a) power loss in two UF3SC120009K4S per switch position, and (b) junction temperatures

Purely reactive power loss and junction temperatures are shown in Figure 9(a) and (b). This is useful to see because it gives an idea of what happens at non-unity power factor, and it can be convenient to use an inductive load for some inverter testing. Except for PWM2, there is quite a difference in power loss distribution with changing power factor.

Focusing on PWM3 and PWM4, if the switching frequency of PWM4 is doubled, so they both have the same apparent frequency (seen by the line filter), PWM4 has about 5% more total loss as PWM3 in rectifier mode (PF = -1), and 13% lower total loss in inverter mode (PF = 1). This brings into question the effectiveness of PWM3 modulation, especially considering its higher control complexity.



(a)



(b)

Figure 10 Inverter mode: (a) power loss in two UF3SC120016K4S per switch position, and (b) junction temperatures

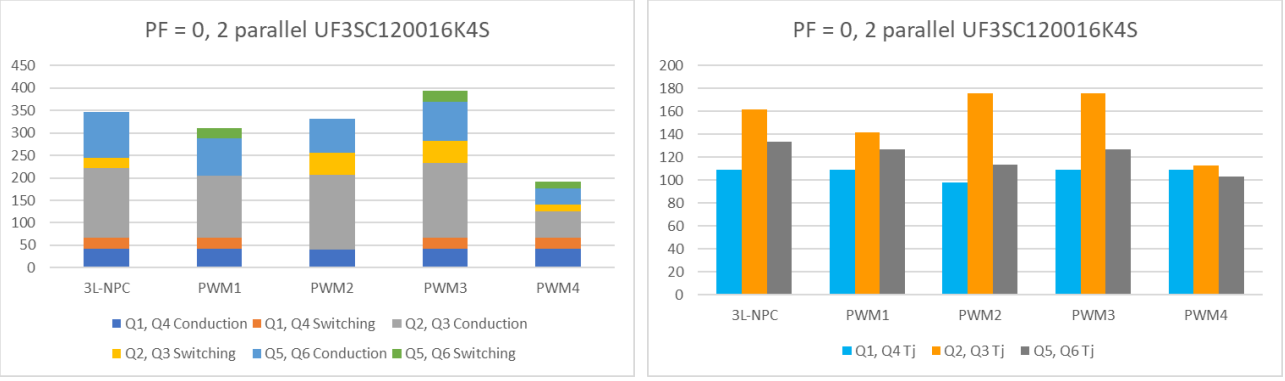
UnitedSiC FETs have a 5 V threshold voltage @ 25 °C, so negative gate drive voltage is optional. This combined with low gate charge help to minimize gate drive cost.

Running the same calculations but changing the FET part number to UF3SC120016K4S again clearly shows the conduction loss advantage of PWM4. Two parallel UF3SC120016K4S should work fine in PWM4 in any operating mode. From Figure 10(b), two parallel UF3SC120016K4S would overheat in switch positions Q2 and Q3 in PWM2 and PWM3. In rectifier mode, the Q2, Q3 FETs overheat in all but PWM1 and PWM4, as seen in Figure 11(b).

These power loss estimates make it clear that the added cost of gate drivers and power supplies for Q5 and Q6 in PWM4 versus 3L-NPC should be easily justified given the substantial efficiency improvement. The flexible gate drive of UnitedSiC FETs can further reduce costs because negative gate drive voltage is optional. A further benefit of PWM4 is its simplicity; Q5 and Q6 are switched the same as Q3 and Q2 respectively, making an easy upgrade path from 3L-NPC.

(a) (b)

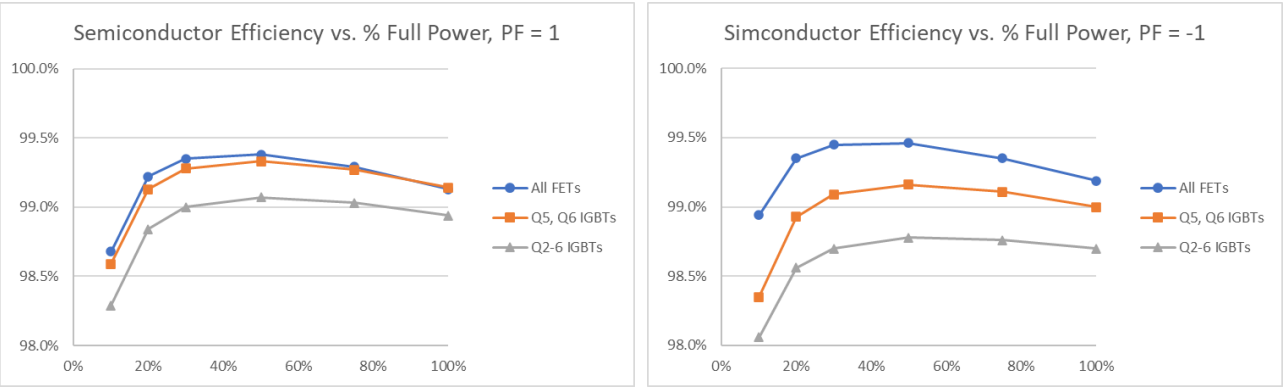
Figure 11 Rectifier mode: (a) power loss in two UF3SC120016K4S per switch position, and (b) junction temperatures



(a) (b)

Figure 12 Reactive mode: (a) power loss in two UF3SC120016K4S per switch position, and (b) junction temperatures

Taking a closer look at PWM4 for an application where the heat sink reaches 100 °C (left to bake out in the summer sun), two parallel UF3SC120009K4S would be needed for Q1 and Q4, while two parallel UF3SC120016K4S will still work for Q2 and Q3. The devices in Q5 and Q6 positions are always more lightly loaded than the others, and the devices in Q2 and Q3 positions are more lightly loaded in inverter mode than in rectifier mode. Power loss in each switch position and semiconductor efficiency at various loading is shown in Figure 13.



(a) (b)

Figure 13 PWM4 combined semiconductor efficiency with T_{sink} = 100 °C, two parallel UF3SC120009K4S per Q1 and Q4 switch positions; two parallel UF3SC120016K4S or two parallel 1200 V, 75 A high speed IGBT per Q2 and Q3; and two parallel UF3C120040K4S or two parallel of the 1200 V, 75 A IGBTs per Q5 and Q6; (a) with PF = 1, and (b) PF = -1

In inverter mode with PF = 1, there is negligible switching loss in Q2, Q3, Q5, and Q6. Therefore, it is interesting to compare efficiency between UnitedSiC FETs and IGBTs in these switch positions. The results of this comparison is shown in Figure 13(a) where Q5 and Q6 devices are replaced with two parallel 1200 V, 75 A high speed IGBTs with co-packaged anti-parallel diodes. Q5 and Q6 switch positions can use either a single UF3SC120016K4S or two parallel UF3C120040K4S; the latter option has the lowest total power loss. In inverter mode, the efficiency with IGBTs in Q5 and Q6 positions is almost the same as with two parallel UF3C120040K4S FETs. If the FETs in Q2 and Q3 positions are replaced with these same type IGBTs, again two in parallel in each switch position, then the overall efficiency drops noticeably.

The same comparison was made for rectifier mode with PF = -1. The results are shown in Figure 13(b). In rectifier mode, the significant switching losses in Q2, Q3, Q5, and Q6 positions degrades the efficiency, bringing into question trying to save a dollar or two with the IGBTs. Another question naturally arises: where are the losses from? A view into this is given in Figure 14 below.

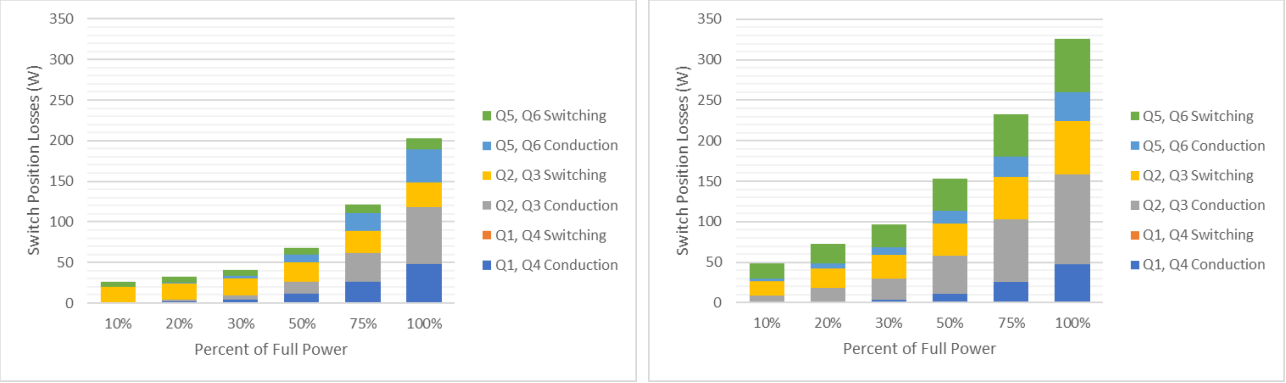


Figure 14 Losses by switch position for PF = -1, two parallel UF3SC120009K4S in Q1 and Q4; and (a) two parallel UF3SC120016K4S in Q2 and Q3, and two parallel UF3C120040K4S in Q5 and Q6; and (b) two parallel 1200 V, 75 A high speed IGBT in Q2, Q3, Q5, and Q6

As expected, the switching loss is much lower with the UnitedSiC FETs, but it is interesting to note that the conduction loss is also significantly lower than for the IGBT in switch positions Q2 and Q3. This highlights the efficiency advantage of FETs in an inverter with the elimination of the "knee voltage" that is present in both the IGBT and its anti-parallel diode.

6 Conclusion

Power loss and efficiency calculations are power tools for quickly evaluating tradeoffs between various circuit topologies and control strategies. This application note compared two topologies and five modulation methods, outlining the basic operation and tradeoffs of each. Power loss calculations were explained, and all formulas are listed in the appendix for reference. The results of calculations for an example 150 kVA inverter show that the added cost of replacing diodes with FETs and their associated gate drive circuitry brings a reduction in semiconductor power loss of up to 34 % when comparing 3L-NPC with ANPC using PWM4 modulation. Doubling the switching frequency with PWM4 modulation was predicted to be about equal or better in efficiency than the apparent frequency doubling of PWM3 modulation. In addition to highest efficiency under all operating modes (any power factor), PWM4 modulation is simple, very similar to 3L-NPC, and switching utilization is especially good in rectifier mode. Comparisons of mixing UnitedSiC FETs and IGBT in different switch positions revealed that IGBTs only in Q5 and Q6 switch positions and only in inverter mode yield comparable efficiency to all-FETs implementations. Otherwise, the UnitedSiC FETs have significantly lower overall power loss. Loss calculations help with device selection and paralleling, saving test time and optimizing cost and performance while simplifying control.

7 References

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8 Appendix

Switch	Conduction Interval	Modulation Function
Q1	(φ, π)	$m \cdot \sin(\theta)$
D1	$(0, \varphi)$	$m \cdot \sin(\theta)$
Q2	(φ, π)	1
	$(\pi, \pi + \varphi)$	$1 + m \cdot \sin(\theta)$
D2	$(0, \varphi)$	$m \cdot \sin(\theta)$
D5	(φ, π)	$1 - m \cdot \sin(\theta)$
	$(\pi, \pi + \varphi)$	$1 + m \cdot \sin(\theta)$

Table 7 3L-NPC conduction loss intervals and modulation functions

Switch	Switching Loss Formula
Q1, D5	$\frac{1}{8\pi}\left[a_{sw} I_{pk}^2 [2(\pi - \varphi) + \sin(2\varphi)] + 4 b_{sw} I_{pk} (1 + \cos(\varphi)) + 4 c_{sw} (\pi - \varphi)\right] \frac{V_{DC}/2}{V_{ref}} f_{sw}$
Q2, D1	$\frac{1}{8\pi}\left[a_{sw} I_{pk}^2 (2\varphi - \sin(2\varphi)) + 4 b_{sw} I_{pk} (1 - \cos(\varphi)) + 4\varphi c_{sw}\right] \frac{V_{DC}/2}{V_{ref}} f_{sw}$
Switch	Switching Loss Interval
Q1, D5	(φ, π)
Q2	$(\pi, \pi + \varphi)$
D1	$(0, \varphi)$

Table 8 3L-NPC switching loss formulas

	Conduction Interval				Modulation Function			
Switch	PWM1	PWM2	PWM3	PWM4	PWM1	PWM2	PWM3	PWM4
Q1	(φ, π)				$m \cdot \sin(\theta)$			
D1	$(0, \varphi)$				$m \cdot \sin(\theta)$			
Q2	(φ, π)	(φ, π)	$(\varphi, \pi + \varphi)$	$(\varphi, \pi + \varphi)$	1	$m \cdot \sin(\theta)$	$\frac{1 + m \cdot \sin(\theta)}{2}$	$1 + m \cdot \sin(\theta)$
		$(\pi, \pi + \varphi)$				$1 + m \cdot \sin(\theta)$		
D2	$(0, \varphi)$	$(0, \varphi)$	$(0, \varphi)$	$(0, \varphi)$	1	$m \cdot \sin(\theta)$	$\frac{1 + m \cdot \sin(\theta)}{2}$	$1 + m \cdot \sin(\theta)$
		$(\pi + \varphi, 2\pi)$	$(\pi + \varphi, 2\pi)$	$(\pi + \varphi, 2\pi)$		$1 + m \cdot \sin(\theta)$	$\frac{1 + m \cdot \sin(\theta)}{2}$	$1 + m \cdot \sin(\theta)$
Q5	$(0, \varphi)$	$(\pi + \varphi, 2\pi)$	$(0, \varphi)$	$(0, \varphi)$	$1 - m \cdot \sin(\theta)$	$1 + m \cdot \sin(\theta)$	$\frac{1 - m \cdot \sin(\theta)}{2}$	$1 - m \cdot \sin(\theta)$
			$(\pi + \varphi, 2\pi)$	$(\pi + \varphi, 2\pi)$			$\frac{1 + m \cdot \sin(\theta)}{2}$	$1 + m \cdot \sin(\theta)$
D5	(φ, π)	$(\pi, \pi + \varphi)$	(φ, π)	(φ, π)	$1 - m \cdot \sin(\theta)$	$1 + m \cdot \sin(\theta)$	$\frac{1 - m \cdot \sin(\theta)}{2}$	$1 - m \cdot \sin(\theta)$
			$(\pi, \pi + \varphi)$	$(\pi, \pi + \varphi)$			$\frac{1 + m \cdot \sin(\theta)}{2}$	$1 + m \cdot \sin(\theta)$

Table 9 3L-ANPC conduction loss intervals and modulation functions

Circuit	Switch	Conduction Loss Formula
NPC	Q1	$\frac{m}{12\pi}\cdot\left[2I_{pk}^2R_{DS}(1+\cos(\varphi))^2+3I_{pk}V_0[(\pi-\varphi)\cos(\varphi)+\sin(\varphi)]\right]$
	D1	$\frac{m}{12\pi}\cdot\left[2I_{pk}^2R_{DS}(1-\cos(\varphi))^2+3I_{pk}V_0[-\varphi\cos(\varphi)+\sin(\varphi)]\right]$
	Q2	$\frac{1}{12\pi}\cdot\left[I_{pk}^2R_{DS}[3\pi-2m(1-\cos(\varphi))^2]+3I_{pk}V_0[4+m(\varphi\cos(\varphi)-\sin(\varphi))]\right]$
	D5	$\frac{1}{12\pi}\cdot\left[I_{pk}^2R_{DS}[3\pi-4m(1+\cos(\varphi))^2]+3I_{pk}V_0[4+m((2\varphi-\pi)\cos(\varphi)-2\sin(\varphi))]\right]$
PWM1	Q1	$\frac{m}{12\pi}\cdot\left[2I_{pk}^2R_{DS}(1+\cos(\varphi))^2+3I_{pk}V_0[(\pi-\varphi)\cos(\varphi)+\sin(\varphi)]\right]$
	D1	$\frac{m}{12\pi}\cdot\left[2I_{pk}^2R_{DS}(1-\cos(\varphi))^2+3I_{pk}V_0[-\varphi\cos(\varphi)+\sin(\varphi)]\right]$
	Q2	$\frac{1}{8\pi}\left[I_{pk}^2R_{DS}[2(\pi-\varphi)+\sin(2\varphi)]+4I_{pk}V_0(1+\cos(\varphi))\right]$
	D2	$\frac{1}{8\pi}\left[I_{pk}^2R_{DS}[2\varphi-\sin(2\varphi)]+4I_{pk}V_0(1-\cos(\varphi))\right]$
	Q5	$\frac{1}{24\pi}\left[I_{pk}^2R_{DS}[6\varphi-3\sin(2\varphi)-4m(1-\cos(\varphi))^2]+6I_{pk}V_0[2(1-\cos(\varphi))+m(\varphi\cos(\varphi)-\sin(\varphi))]\right]$
	D5	$\frac{1}{24\pi}\left[I_{pk}^2R_{DS}[6(\pi-\varphi)+3\sin(2\varphi)-4m(1+\cos(\varphi))^2]+6I_{pk}V_0\left[2(1+\cos(\varphi))+m\left((\varphi-\pi)\cos(\varphi)-\sin(\varphi)\right)\right]\right]$
PWM2	Q1	$\frac{m}{12\pi}\cdot\left[2I_{pk}^2R_{DS}(1+\cos(\varphi))^2+3I_{pk}V_0[(\pi-\varphi)\cos(\varphi)+\sin(\varphi)]\right]$
	D1	$\frac{m}{12\pi}\cdot\left[2I_{pk}^2R_{DS}(1-\cos(\varphi))^2+3I_{pk}V_0[-\varphi\cos(\varphi)+\sin(\varphi)]\right]$
	Q2	$\frac{1}{24\pi}\left[I_{pk}^2R_{DS}[3(2\varphi-\sin(2\varphi))+16m\cos(\varphi)]+6I_{pk}V_0[2(1-\cos(\varphi))+\pi m\cos(\varphi)]\right]$
	D2	$\frac{1}{24\pi}\left[I_{pk}^2R_{DS}[6(\pi-\varphi)+3\sin(2\varphi)-16m\cos(\varphi)]+6I_{pk}V_0[2(1+\cos(\varphi))-\pi m\cos(\varphi)]\right]$
	Q5	$\frac{1}{24\pi}\left[I_{pk}^2R_{DS}[6(\pi-\varphi)+3\sin(2\varphi)-4m(1+\cos(\varphi))^2]+6I_{pk}V_0\left[2(1+\cos(\varphi))+m\left((\varphi-\pi)\cos(\varphi)-\sin(\varphi)\right)\right]\right]$
	D5	$\frac{1}{24\pi}\left[I_{pk}^2R_{DS}[6\varphi-3\sin(2\varphi)-4m(1-\cos(\varphi))^2]+6I_{pk}V_0[2(1-\cos(\varphi))+m(\varphi\cos(\varphi)-\sin(\varphi))]\right]$
PWM3	Q1	$\frac{m}{12\pi}\cdot\left[2I_{pk}^2R_{DS}(1+\cos(\varphi))^2+3I_{pk}V_0[(\pi-\varphi)\cos(\varphi)+\sin(\varphi)]\right]$
	D1	$\frac{m}{12\pi}\cdot\left[2I_{pk}^2R_{DS}(1-\cos(\varphi))^2+3I_{pk}V_0[-\varphi\cos(\varphi)+\sin(\varphi)]\right]$
	Q2	$\frac{1}{24\pi}\left[I_{pk}^2R_{DS}(3\pi+8m\cos(\varphi))+3I_{pk}V_0(4+\pi m\cos(\varphi))\right]$
	D2	$\frac{1}{24\pi}\left[I_{pk}^2R_{DS}(3\pi-8m\cos(\varphi))+3I_{pk}V_0(4-\pi m\cos(\varphi))\right]$
	Q5, D5	$\frac{1}{24\pi}\cdot\left[I_{pk}^2R_{DS}[3\pi-4m(1+\cos(\varphi)^2)]+3I_{pk}V_0[4+m((2\varphi-\pi)\cos(\varphi)-2\sin(\varphi))]\right]$
PWM4	Q1	$\frac{m}{12\pi}\cdot\left[2I_{pk}^2R_{DS}(1+\cos(\varphi))^2+3I_{pk}V_0[(\pi-\varphi)\cos(\varphi)+\sin(\varphi)]\right]$
	D1	$\frac{m}{12\pi}\cdot\left[2I_{pk}^2R_{DS}(1-\cos(\varphi))^2+3I_{pk}V_0[-\varphi\cos(\varphi)+\sin(\varphi)]\right]$
	Q2	$\frac{1}{48\pi}\left[I_{pk}^2R_{DS}(3\pi+8m\cos(\varphi))+6I_{pk}V_0(4+\pi m\cos(\varphi))\right]$
	D2	$\frac{1}{48\pi}\left[I_{pk}^2R_{DS}(3\pi-8m\cos(\varphi))+6I_{pk}V_0(4-\pi m\cos(\varphi))\right]$
	Q5, D5	$\frac{1}{48\pi}\cdot\left[I_{pk}^2R_{DS}[3\pi-4m(1+\cos(\varphi)^2)]+6I_{pk}V_0[4+m((2\varphi-\pi)\cos(\varphi)-2\sin(\varphi))]\right]$

Table 10 3L-NPC and 3L-ANPC conduction loss formulas for various modulation strategies

Switch	Switching Loss Formula
Q1, D5	$\frac{1}{8\pi}\left[a_{sw}I_{pk}^2[2(\pi-\varphi)+\sin(2\varphi)]+4b_{sw}I_{pk}(1+\cos(\varphi))+4c_{sw}(\pi-\varphi)\right]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
Q2, D2	0
Q5, D1	$\frac{1}{8\pi}\left[a_{sw}I_{pk}^2(2\varphi-\sin(2\varphi))+4b_{sw}I_{pk}(1-\cos(\varphi))+4\varphi c_{sw}\right]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
Switch	Switching Loss Interval
Q1, D5	(φ,π)
Q5, D1	$(0,\varphi)$

Table 11 3L-ANPC PWM1 switching loss formulas

Switch	Switching Loss Formula
Q1, Q5, D1, D5	0
Q2, D2	$\frac{1}{8\pi}\left(2a_{sw}\pi I_{pk}^2+8b_{sw}I_{pk}+4\pi c_{sw}\right)\frac{V_{DC}/2}{V_{ref}}f_{sw}$
Switch	Switching Loss Interval
Q2	$(\varphi,\pi+\varphi)$
D2	$(\pi+\varphi,2\pi+\varphi)$

Table 12 3L-ANPC PWM2 switching loss formulas

Switch	Switching Loss Formula
Q1, D5	$\frac{1}{8\pi}\left[a_{sw}I_{pk}^2[2(\pi-\varphi)+\sin(2\varphi)]+4b_{sw}I_{pk}(1+\cos(\varphi))+4c_{sw}(\pi-\varphi)\right]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
Q2, D2	$\frac{1}{8\pi}\left(2a_{sw}\pi I_{pk}^2+8b_{sw}I_{pk}+4\pi c_{sw}\right)\frac{V_{DC}/2}{V_{ref}}f_{sw}$
Q5, D1	$\frac{1}{8\pi}\left[a_{sw}I_{pk}^2(2\varphi-\sin(2\varphi))+4b_{sw}I_{pk}(1-\cos(\varphi))+4\varphi c_{sw}\right]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
Switch	Switching Loss Interval
Q1, D5	(φ,π)
Q2	$(\varphi,\pi+\varphi)$
Q5, D1	$(0,\varphi)$
D2	$(\pi+\varphi,2\pi+\varphi)$

Table 13 3L-ANPC PWM3 switching loss formulas

Switch	Switching Loss Formula
Q1	$\frac{1}{8\pi}\left[a_{sw}I_{pk}^2[2(\pi-\varphi)+\sin(2\varphi)]+4b_{sw}I_{pk}(1+\cos(\varphi))+4c_{sw}(\pi-\varphi)\right]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
Q2, Q5	$\frac{1}{32\pi}\left[a_{sw}I_{pk}^2(2\varphi-\sin(2\varphi))+8b_{sw}I_{pk}(1-\cos(\varphi))+16\varphi c_{sw}\right]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
D1	$\frac{1}{8\pi}\left[a_{sw}I_{pk}^2(2\varphi-\sin(2\varphi))+4b_{sw}I_{pk}(1-\cos(\varphi))+4\varphi c_{sw}\right]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
D2, D5	$\frac{1}{32\pi}\left[a_{sw}I_{pk}^2[2(\pi-\varphi)+\sin(2\varphi)]+8b_{sw}I_{pk}(1+\cos(\varphi))+16c_{sw}(\pi-\varphi)\right]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
Switch	Switching Loss Interval
Q1, D5	(φ,π)
Q2	$(\pi,\pi+\varphi)$
Q5, D1	$(0,\varphi)$

Table 14 3L-ANPC PWM4 switching loss formulas