APPLICATION NOTE
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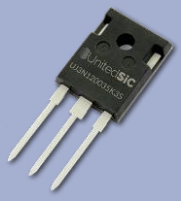
Gate Drive and Protection of Three-Level Inverters

By Jonathan Dodge, P.E.

Introduction

There are multiple variants of three-level neutral point clamped inverters. Most are derivatives of two circuit topologies: one with four series-connected FETs and two clamp diodes, the other with two series-connected FETs and two clamp FETs. The first one is diode neutral point clamped but simply called neutral point clamped (NPC). The second one is transistor neutral point clamped (TNPC), and the phase leg schematic resembles a sideways letter T. There are different tradeoffs between these two topologies, but in the end the gate drive requirements and implementation are very similar. Of concern is how to safely drive and control the series-connected FETs as well as how to handle fault conditions, including a short circuit. This is explained in this note, in addition to a discussion of overall operation and how it relates to gate driving.

Jonathan Dodge is a Senior Applications Engineer at United Silicon Carbide. Experience includes design of analog, digital, and power electronics; working with power levels ranging from 1.5 to 500 kW in renewable energy and other applications.



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Three-Level Topologies and Switch States

UnitedSiC cascode FETs are a good choice for hard-switched inverters due to the low on-resistance, low reverse recovery charge, and flexible gate drive.

Three-level inverters have a split DC link so that each AC output can connect to three potentials: DC+, DC- and the neutral point N, which is the center point of the DC link. Freewheeling current paths are provided to clamp the output to the neutral point, allowing the three-level inverter to operate at any power factor. The clamping is done by the combination of a diode and a FET that is on (conducting in the forward direction). The FETs mentioned here are UnitedSiC cascode. Inherent in the cascode is automatic reverse conduction whether the gate is on or off, similar to a MOSFET. Therefore, in the following circuit diagrams the intrinsic diode feature is not labelled separately from the FETs.

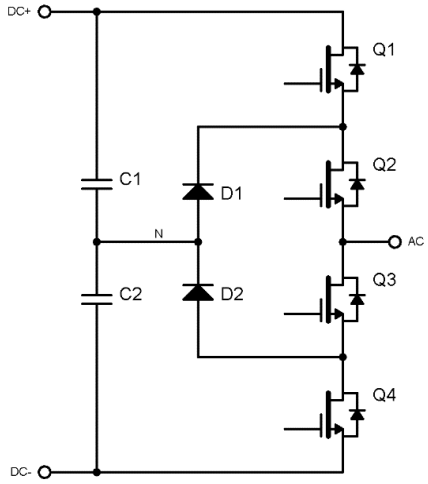


Figure 1 NPC phase leg

In the NPC topology of Figure 1 the clamp function is performed by Q2 with D1, and Q3 with D2. Four FETs are connected in series, and therefore care must be taken to avoid a shoot-through condition. This is straightforward with the following two rules:

1. Q1 always switches opposite of Q3, and Q4 always switches opposite of Q2. Stated another way, interlock with deadtime between Q1 and Q3, as well as between Q4 and Q2 always prevents a shoot-through condition.
2. Q1 and Q4 cannot be on simultaneously.

It is worthwhile to consider why these two rules always result in safe operation. In the NPC topology, the FETs and diodes are required to block the voltage across only one of the DC link capacitors, which have nearly equal voltage across them. Therefore, the voltage rating of the FETs and diodes can be half that required to block the entire DC link voltage. This is an advantage of the NPC topology because of the higher efficiency of lower voltage-rated FETs, or the ability to operate at higher DC link voltage.

State	Safe						Hazardous					Destructive				
Q1	0	0	0	0	1	0	1	0	1	1	0	1	1	1	0	1
Q2	0	1	0	1	1	0	0	0	0	0	1	1	1	0	1	1
Q3	0	0	1	1	0	1	0	0	0	1	0	1	0	1	1	1
Q4	0	0	0	0	0	1	0	1	1	0	1	0	1	1	1	1

Table 1 NPC switch states

A voltage rating lower than the total DC link voltage means there could be some hazardous states, depending on the switch states of the other phase legs in the inverter [1]. All possible NPC phase leg switch states are shown in Table 1. Hazardous states include either or both Q1 or Q4 switched on, and non-adjacent FETs switched on. These states can cause an overvoltage across a FET and/or diode. Destructive states short the upper, lower, or both DC link halves. No matter what direction the current flows in the AC terminal, the safe states cannot cause a device overvoltage. The safe states include all off, either or both inner FETs switched on, and any two adjacent FETs switched on. It is clear from Table 1 that both safety rules mentioned above are followed in the safe switch states, but they are not followed in the hazardous and destructive states.

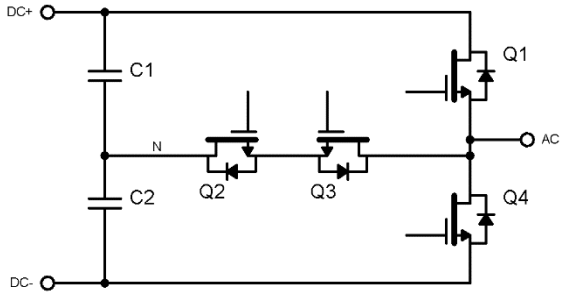


Figure 2 TNPC phase leg with commom-source clamp FETs

The common-drain clamp FET configuration requires the fewest isolated gate drive power supplies.

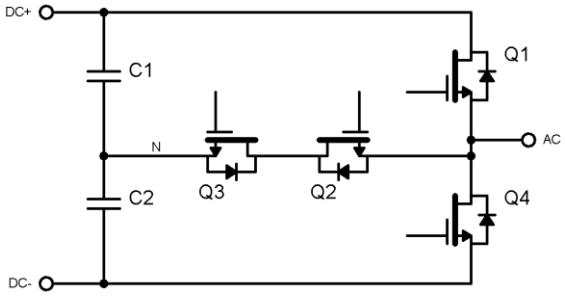


Figure 3 TNPC phase leg with common-drain clamp FETs

In the TNPC topology of Figure 2 and Figure 3 the clamp function is performed by Q2 and Q3, with obviously reverse current flowing through one (therefore acting as a diode), and forward current through the other. Q1 and Q4 must block the full DC link voltage, just as in a two-level inverter. The clamp FETs block the voltage across only one of the DC link capacitors, and therefore the voltage rating of these FETs can be half that required to block the entire DC link voltage. An advantage of the TNPC topology is its similarity and hence familiarity to a two-level inverter. It has the same output waveforms as the NPC topology but can operate at only half the total DC link voltage, given the same voltage rated FETs. The difference between Figure 2 and Figure 3 is the clamp FETs are connected common-source and common-drain respectively. The functionality of both is the same, and the same two safety rules apply as for the NPC topology.

State	Safe								Destructive							
Q1	0	1	0	0	0	1	0	0	1	1	0	1	1	1	0	1
Q2	0	0	1	0	0	1	1	0	0	0	1	1	1	0	1	1
Q3	0	0	0	1	0	0	1	1	0	1	0	1	0	1	1	1
Q4	0	0	0	0	1	0	0	1	1	0	1	0	1	1	1	1

Table 2 TNPC switch states

In the TNPC there are no hazardous switch states, only safe or destructive. All possible TNPC phase leg switch states are shown in Table 2. The astute reader will notice that there are two more safe states compared to NPC, namely Q1 or Q4 can be switched on while all other FETs are off. These state however are not necessary, nor are they normal operating states as will be shown. Destructive states include Q1 and Q4 switched on, which shorts the entire DC link, and any combination of non-adjacent FETs switched on, which shorts one or both halves of the DC link. Again, it is clear from Table 2 that both safety rules are followed in the safe switch states, but they are not followed in the destructive states.

Control of AC Terminal Voltage

The question naturally arises of whether the AC terminal voltage can always be controlled while following the safety rules, regardless of the polarities of the AC terminal voltage and current. Consider current leaving the AC terminal to be positive. There are four cases to consider:

1. Positive current with Q4 remaining off, Q2 remaining on, while Q1 and Q3 alternate switch states
2. Negative current with Q4 remaining off, Q2 remaining on, while Q1 and Q3 alternate switch states
3. Negative current with Q1 remaining off, Q3 remaining on, while Q4 and Q2 alternate switch states
4. Positive current with Q1 remaining off, Q3 remaining on, while Q4 and Q2 alternate switch states

In the first case, current commutates between Q1 and D1 in NPC, and between Q1 and Q3 in TNPC, and the AC terminal voltage toggles between DC+ and N when Q1 switches on and off respectively (and Q3 switches the opposite). In the second case, commutation is between Q1 – Q2 and D2 – Q3 in NPC, and in TNPC it is still between Q1 and Q3. Again, the AC terminal voltage toggles to DC+ whenever Q1 is on, and to N whenever Q1 is off (with Q3 the opposite). The analysis is similar for the other two cases, only with opposite voltage and current polarities. In all cases, the AC terminal voltage is controlled, and therefore, more switch states are not needed. This also means that the same control strategy works for TNPC as for NPC.

State Transition Diagram

Because FETs cannot switch instantaneously on and off (although they come close to it), some deadtime must be added. This means that there are times when only one FET in a phase leg is switched on at a time. From at Table 1, the NPC inner FETs Q2 and Q3 must always be switched on first and off last. This is not a requirement for TNPC, and this is an important difference between the topologies regarding emergency shutdown.

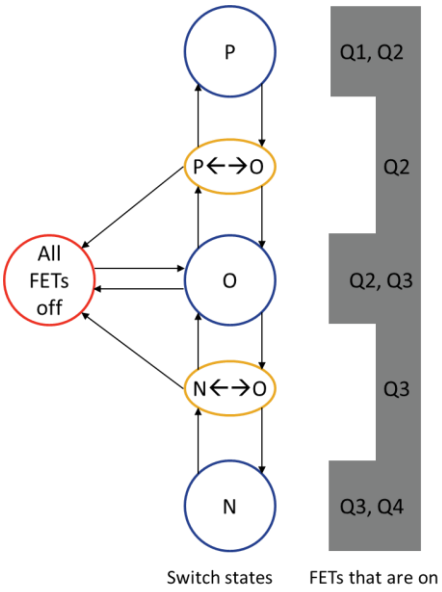


Figure 4 State transition diagram

We name some switch states to make a simple state diagram as shown in Figure 4 where the P state represents Q1 and Q2 switched on, N has Q3 and Q4 on, O has Q2 and Q3 on, and in the Off state all FETs are switched off [2]. Each of the two remaining states represents a transition during a deadtime. The arrows in Figure 4 show the allowable state transitions. Following these ensures that both NPC and TNPC inverters are always in a safe state, even while switching. At first glance it may seem complicated to always follow this state transition diagram, but it is actually straightforward.

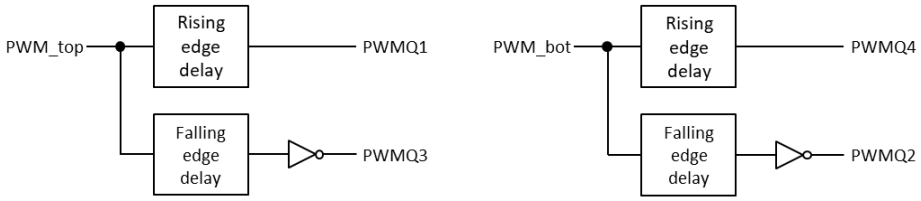


Figure 5 Deadband and interlock generation

A pulse width modulation (PWM) peripheral in a microcontroller can generate PWM outputs to control each FET with interlock and deadtime. Alternatively, many half-bridge gate drivers include interlock and deadtime features. A block diagram representation of an interlock and deadtime implementation is shown in Figure 5. In a microcontroller such as one from the C2000™ series from Texas Instruments, the edge delays are generated with programmable counters. In a half-bridge gate driver, the delays are typically programmable by changing a capacitor value on the circuit board. The interlock is done by digital inversion. In any case, two PWM signals can control a three-level phase leg by adding interlock and deadtime.

PWM_top	PMW_bot	States
0	0	Off, P←→O, or N←→O to O
0	1	P←→O to P
1	0	N←→O to N
1	1	Disallowed

Table 3 Possible states and transitions based on PWM generator outputs

In Figure 5, the PWM signal PWM_top controls FETs Q1 and Q3; PWM signal PWM_bot controls FETs Q4 and Q2. The signals PWM_top and PWM_bot can be generated either by double-carrier [3] or space vector methods [4]. Table 3 maps all combinations of the digital signals PWM_top and PWM_bot to the state diagram in Figure 4. Note that a three-level PWM generator never simultaneously toggles PWM_top and PWM_bot, which would be two-level operation; and it never generates the disallowed state where both are 1 for the same reasons a two-level PWM generator would never command the top and bottom FETs in a leg to be on simultaneously. This is an inherent feature of PWM generation algorithms, whether carrier-based or space vector, and it greatly simplifies following the state diagram in Figure 4 and hence adhering to the two safety rules.

Before startup or after shutdown, all FETs can be kept off by overriding the signals PWMQ1 through PWMQ4 in Figure 5 while PWM_top and PWM_bot are both kept at 0. This can be accomplished for example by disconnecting the PWM peripheral and directly driving the microcontroller I/O pins, or by asserting disable signals to half-bridge gate drivers. Upon connecting the PWM peripheral to the I/O pins or enabling the gate drivers, the state transitions from all FETs off to the inherently safe O state, with Q2 and Q3 switched on. From here, state transitions are between O and P, or O and N through the respective deadtime states P←→O and N←→O.

The only remaining concern is the shutdown sequence, for which the controller sets both PWM_top and PWM_bot to 0 for at least one deadtime before directly driving the I/O pins or by asserting gate driver disable signals. This sequence should be followed for both normal and emergency shutdown, at least for the NPC topology. In TNPC Q1 and Q4 can block the entire DC link voltage, and therefore all FETs can be safely switched off simultaneously.

To summarize, the state transition diagram is followed by using interlock and deadtime between FET pairs Q1 – Q3, and Q4 – Q2, by starting in the O state, and by switching off Q1 and Q4 (go toward the O state) at least one deadtime period before all FETs are switched off.

Figure 6 and Figure 7 below show an example of gate control signal generation using the PWM peripheral of a TMS320F28335 microcontroller. The waveforms are labelled Q1 through Q4 corresponding to the FETs in Figure 1, Figure 2, or Figure 3. Two internal PWM signals are generated. Rising and falling edge delays are added to each. The signals with rising edge delays drive Q1 and Q4, while the signals with falling edge delays are inverted and drive Q3 and Q2, as indicated in Figure 5.

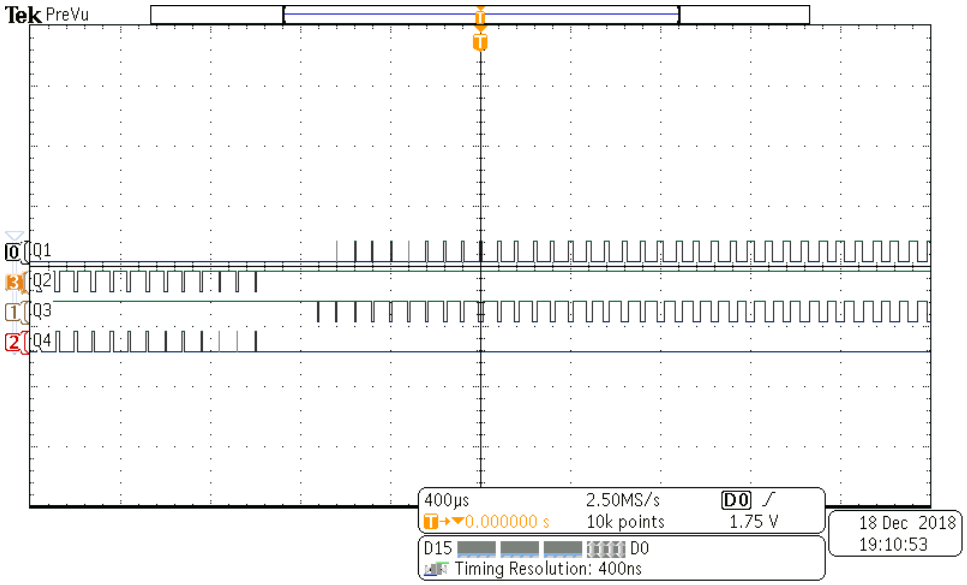


Figure 6 Gate control signal generation with a microcontroller

In Figure 6, the average AC terminal voltage transitions from negative to positive. Initially Q1 remains off while Q3 remains on, and Q2 switches opposite of Q4. This is typical of three-level inverter operation; pairs of FETs switch during only half the fundamental line cycle. After the average voltage zero-crossing, Q3 switches opposite Q1, and Q4 remains off with Q2 on.

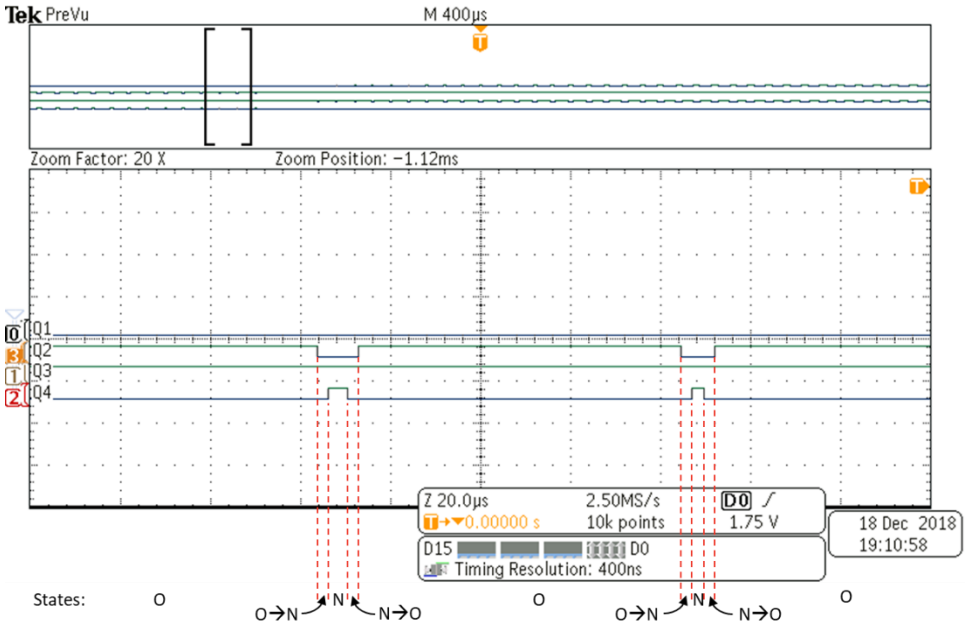


Figure 7 Gate control signals and state transitions

Figure 7 shows a zoomed-in view of Figure 6. The deadtime was increased 10x more than typical to more clearly show the state transitions. This view is when the average AC output is still slightly negative, and the state transitions between O and N through the deadtime state N←→0. From inspection of Figure 6 and Figure 7, it is clear that the state transitions of Figure 4 are followed, and hence the phase leg operates safely.

Overcurrent, DESAT, and Emergency Shutdown

Following are some general guidelines regarding overcurrent protection and DESAT (desaturation) detection for short-circuit protection.

1. Overcurrent detection should be as close as possible to the devices being protected.
2. DESAT is only useful for short-circuits and is not suitable for overcurrent detection.

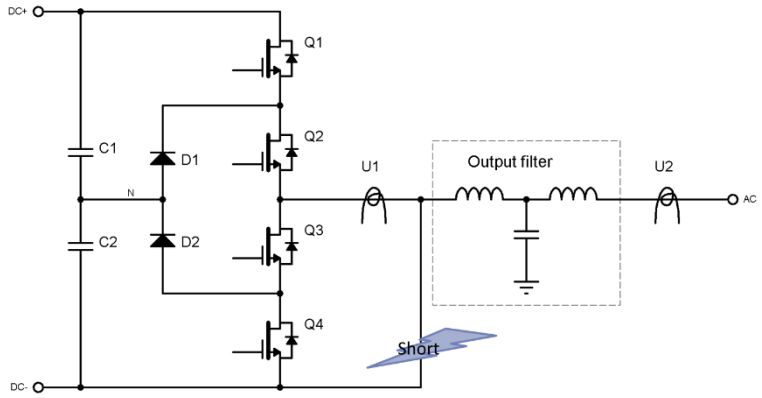


Figure 8 Fault condition and current sense locations

Current at the grid connection point is typically what an inverter must control, and so it is desirable to sense this current for feedback control. This creates a dilemma for using this sensor for overcurrent protection of the FETs. The current sensor labeled U2 in Figure 8 is at the grid connection point, "downstream" of the inverter's output filter, and there is a short fault between the phase leg output and DC-. SiC FETs require very fast short circuit detection if they can survive it at all, but it would be difficult to quickly detect this fault with current sensor U2. Current sensor U1 directly at the output of the phase leg could detect excessive current before fault current can reach a catastrophic level. This example illustrates the advantage of placing current sensing as close as possible to the FETs to protect them from overcurrent.

If a short fault develops upstream of U1, it can be from violating a safe switch state in Table 1 or Table 2, or if one of the FETs already failed short. A physical fault developing here is increasingly unlikely the closer the current sensor is to the FETs. For these reasons, DESAT should be considered a final effort to save a power converter from further damage, but it is likely already damaged.

The noise generated while switching is huge. Two parameters can be adjusted to ignore this noise: blanking time and DESAT threshold voltage. With fast-switching SiC FETs, the blanking time must be kept short, in the range of 3 µs. It is very difficult to get DESAT detection to work *reliably* in less time. The threshold voltage is often set by the gate driver IC, typically 7 to 9 V. There is no need to reduce this threshold by adding diodes or other components in the DESAT detection circuit. Since DESAT threshold voltage and blanking time are a mutual tradeoff, it is desirable to have the threshold voltage as high as possible to avoid false DESAT trips.

With Q1 and Q2 in Figure 8 switched on, the entire DC link is shorted through them. If DESAT of Q1 is detected, then its gate driver can immediately switch it off and notify the controller of the fault. The controller can subsequently switch off Q2 and keep Q4 and Q3 off, which is a safe shutdown sequence. DESAT detection with automatic switch-off of Q2 would cause it to switch off before Q1, resulting in a hazardous switch state due to possible overvoltage of Q2. Notice in the NPC topology that the entire DC link can only be shorted if both Q1 and Q2 are

switched on, whereas in TNPC it can be with only Q1 switched on. If Q2 is switched on, then the lower DC link is shorted for both NPC and TNPC. Q2 can be switched off before Q1 in TNPC because the clamp FETs only block the voltage of the upper or lower DC link halves, never both simultaneously, and Q1 and Q4 must be rated to block the entire DC link voltage.

Referring again to Figure 8, with Q1 off and Q2 on, whether Q3 is on or off, the lower DC link is shorted through D1 and Q2. In this situation it would be safe to detect DESAT of Q2 and automatically switch it off. It can be argued that DESAT detection is only required for Q1 and Q4 [5], with the caveat that the fault condition in Figure 8 would require Q1 to turn on before detection.

If necessity is the mother of invention, then there should be some offspring of three-level specific gate drivers with the following features:

1. One channel isolated gate driver with DESAT detection and fault notification to the controller, with the option to keep the FET on until the controller commands it off, switch it off after a deadtime, or to immediately switch it off. In each case, soft turn-off (higher than normal gate resistance) is used to avoid an overvoltage transient.
2. Dual channel isolated gate driver with DESAT detection and notification on both channels, but one channel always switches off first, then the other channel either after a deadtime period or as commanded by the controller. Both channels would use soft turn-off if either channel detects DESAT.

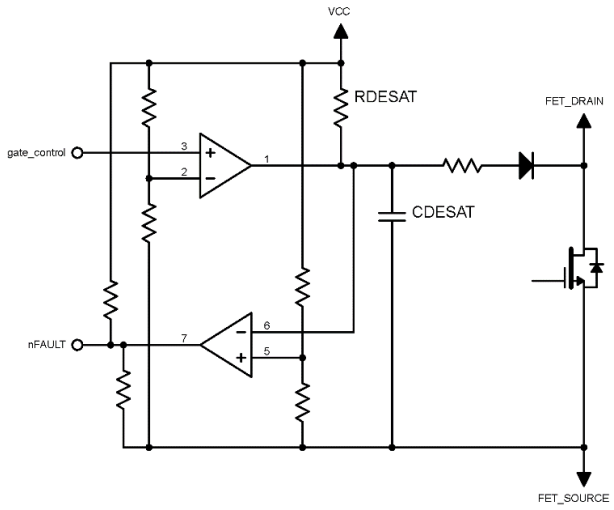
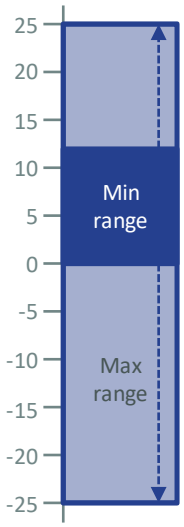


Figure 9 Example of a DESAT detection circuit

An example of a "homemade" DESAT detection circuit is shown in Figure 9. Here the gate control signal that also controls the gate driver (not shown for clarity) connects to the positive input of a comparator. When the gate drive signal is asserted, the open-collector output of the comparator allows RDESAT to charge the capacitor CDESAT. There is an RC charging curve for CDESAT, which provides the DESAT blanking time. The voltage across CDESAT is equal to the drain-source voltage of the FET, plus a small forward voltage across the isolation diode and its recovery surge limiting resistor in series with it. This resistor typically has a value in the range of 100 Ω to 1 kΩ. A second comparator provides the DESAT threshold voltage and trips if the CDESAT voltage is too high. When the gate control signal is off, CDESAT is reset by the first comparator. The comparators could use the gate driver power supply. Not shown are the required signal isolators and noise suppression capacitors, and an optional clamp Schottky

diode across CDESAT. Such a circuit could be used to detect DESAT for a clamp FET in an NPC inverter leg. After isolation, the nFAULT signal could be connected to an input in the controller and/or in gate drivers that immediately switches off all outer FETs in each phase leg, and all remaining FETs would be switched off after a short delay. Alternatively, two isolated gate drivers could be used, one with DESAT detection and built-in fault signal isolation; another without DESAT but that drives the gates of the clamp FET as commanded by the controller.



UnitedSiC cascode gate drive voltage range is from 0/12 V to ±25 V, so they are compatible with gate drivers for other FET types including IGBTs and SiC MOSFETs.

Gate Drive Voltage and Power Supplies

The ability to drive the FET gates with positive-only voltage is a significant advantage of UnitedSiC cascodes in three-level inverters. The typical 5 V gate threshold eliminates the need for a negative gate drive voltage. Bootstrap power supplies can be used for cost savings but note that a large capacitance is required to sustain the gate voltage during half an AC line cycle, during which time a clamp FET must remain on. If using isolated gate drive power supplies in a three-phase inverter, nine supplies are required for NPC, six for TNPC of Figure 2, and only four for TNPC of Figure 3 (one referenced to the shared neutral point, and one to the sources of Q1 and Q2 switch positions in each leg).

Summary

Both three-level NPC and TNPC topologies yield reduced switching loss and harmonic noise compared to two-level inverters. The NPC topology allows operation at higher voltage because the blocking voltage is halved for each power semiconductor, otherwise TNPC is the topology of choice for its lower cost gate drive. The efficiency of each with SiC FETs is very similar [6]. Analysis of safe switch and transition states reveals that both NPC and TNPC can be safely controlled by a microcontroller and/or dual gate drivers with interlock and deadtime generation features. Care must be taken to switch off the outer FETs of NPC before the inner clamp FETs, and in so doing the same controller can be used for both NPC and TNPC topologies. An analysis of a fault condition reveals the need for three-level specific gate driver features. UnitedSiC FETs simplify gate drive power supply requirements be eliminating the need for negative gate drive voltage.

References

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