APPLICATION NOTE

UnitedSiC_AN0018 – November 2018

Switching Fast SiC FETs with a Snubber

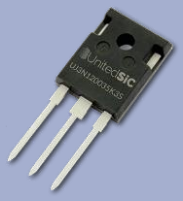
By Mike Zhu

1. Introduction

The emergence of fast switching WBG devices has dramatically enhanced power density in a range of power conversion circuits such as active rectifiers, LLC bridges, Phase shifted full bridges, Dual active bridges to name a few. These circuits form the backbone of efficient AC-DC and DC-DC stages in battery chargers for EVs, forklifts, solar inverters and power supplies, especially where power density is key. The fast switching enabled by these devices is best exploited in advanced packages such as TO247-4L, D2PAK-7L which have a Kelvin Gate Return. However, there are often supply-chain reasons why users are constrained to use standard packages like TO247-3L, TO220-3L and D2PAK-3L, which has high levels of common source inductance.

UnitedSiC has pioneered the introduction of SiC JFET based cascodes with easy drop in compatibility with Si MOSFETs, IGBTs as well as SiC MOSFETs, based on the 5V threshold voltage and wide gate operating range of +/-25V. These devices are inherently very fast switching, with excellent body diode characteristics. However, that also means that operating di/dts can be extremely high. To offer customers various options, the UJ3C series has been created with slower switching speeds, which has higher losses but is easier to use in older 3-leaded packages. Furthermore, a faster UF3C series is being introduced in packages with Kelvin gate returns, such as TO247-4L and D2PAK-7L that offer the highest level of switching performance. For customers

Mike Zhu is an Application Engineer at United Silicon Carbide. Experience includes design of power electronics, EMI mitigation, power device evaluation.



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that need to stay with standard three leaded packages such as TO247-3L, D2PAK-3L and TO220-3L, but still require lower losses in hard switched circuits than the UJ3C series, UnitedSiC offers the UF3C series designed to be used with small RC snubbers to manage the high turn-off di/dts.

Wide-bandgap (WBG) FETs bring a new twist to the well-known RC snubber. Since the devices have very low output capacitance Coss, relatively small values of snubber capacitance are shown to have a large impact on improving overshoots, suppressing gate oscillations and improving EMI. Snubber loss is measured and shown to be much smaller than $f.CV^2$ [1] which is explained in the literature. As switching dV/dt increases, snubber losses increase, but it is also possible to use a smaller snubber to compensate.

In fact, it is found that a 3-5% increase in switching Eon+Eoff loss is enough to dramatically improve switching waveforms. The power loss in the snubber is therefore small enough for surface mount components rated for 0.25W to 2W. We also show that using a snubber simplifies the design effort in making the design compatible with many SiC switch manufacturers, and makes the designs, especially those in highly paralleled configurations, more tolerant of layout issues. The board space for such a snubber can be quite beneficial to ensure that EMI can be reduced at the source if needed, without forcing a major re-design and causing product release delays.

This application note presents the benefits of using an RC snubber connected between the drain and source of fast switching SiC devices in typical applications based on a half-bridge configuration. The challenge of suppressing excessive voltage overshoots and ringing noise is addressed. While the optimization of PCB layouts to reduce parasitic inductance can help, this may often not be possible due to board constraints or product release schedules. Moreover, the common approach to control switching speed from higher gate resistance increases switching loss and delay times. Therefore, this application note presents a practical solution using RC snubbers with fast switching SiC devices. The solution is verified by experimental double pulse tests (DPT) results. The snubber loss is measured very precisely, to assist users compute the power rating of the snubber resistor. The beneficial impact of the snubber is analyzed for both hard switching and soft switching applications. This information has led to the creation of a simple user guide [2].

2. Snubber Loss

A typical RC snubber configuration in a half-bridge is shown in Figure 1. It has a snubber capacitor (Cs) and a snubber resistor (Rs) in series. Load inductor L represents inductive load. The DC LINK capacitor has high capacitance to maintain DC bus voltage while providing energy to the load inductor L. Cd is the power loop decoupling capacitor, usually a ceramic capacitor. It is located close to the half-bridge to minimize power loop inductance during switching transients. CT is a current transformer.

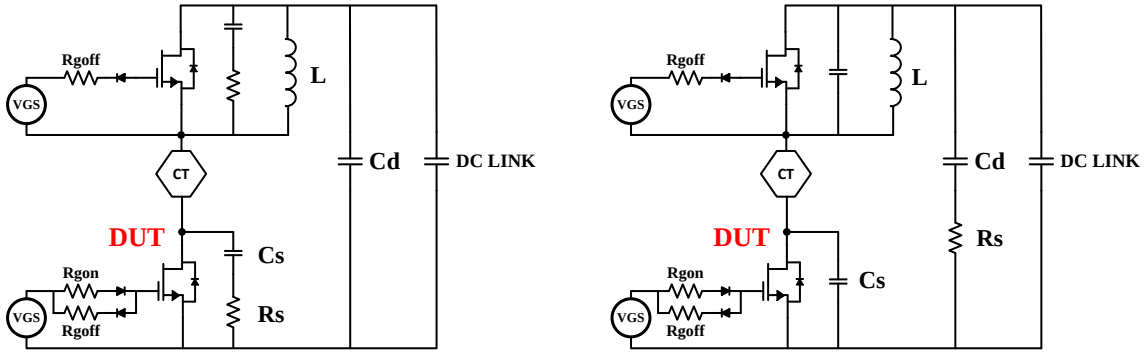


Figure 1. DPT schematic with RC snubbers on both switches for hard switching (a) and soft switching (b).

There are two major concerns with using a basic RC snubber. One is the extra switching energy loss. The other one is the power rating of the snubber resistor Rs. The Snubber Cs will introduce extra turn-on loss (Eon), while reducing turn-off loss(Eoff). When the low side FET (DUT) in the double pulse circuit turns on, the displacement currents charging the high side Cs and discharging the low side Cs create additional loss in the DUT, which depends on the size of the capacitors Cs relative to the FET Coss. During turn-off, the displacement current as the dV/dt rises diverts current from the FET to the Cs-Rs path, reducing the overlap losses in the FET.

Now if a snubber is not used, the SiC device needs to be substantially slowed down to prevent VDS spikes and ringing during the turn-off transient. However, as shown in section 4 the UF3C120040K3S with snubber has the lowest overall loss. In other words, to reach high efficiency and damp ringing the increase of energy loss by switching faster FETs with a snubber is less than that of switching devices slower without a snubber. With a proper snubber design, high switching speed, high efficiency and smooth waveforms can be simultaneously achieved.

For soft switching applications like LLC and PSFB the Cs energy is recycled during zero voltage switching (ZVS). Also, soft switching tends to have high switching frequencies. Therefore, a snubber Rs is not recommended. For supplying inductive loads with a half-bridge configuration like in Fig. 1, the low side turn-off dV/dt will introduce a discharging current in high side snubber

Cs which will reduce the low side turn-off current thus reducing Eoff. Results in section 5 shows that Cs can help reducing turn-off loss (Eoff).

Article [1] explains the difference of Rs loss calculation between ideal square VDS waveforms and practical VDS waveforms with a finite rise time. The common practice of $f \cdot CV^2$ overestimates the loss in a snubber resistor quite a lot. This is because in a practical VDS waveform the snubber Cs is not charging or discharging at a constant voltage. The operating dV/dt has a strong effect on the accuracy of $f \cdot CV^2$ estimation, so it is best to measure snubber loss directly.

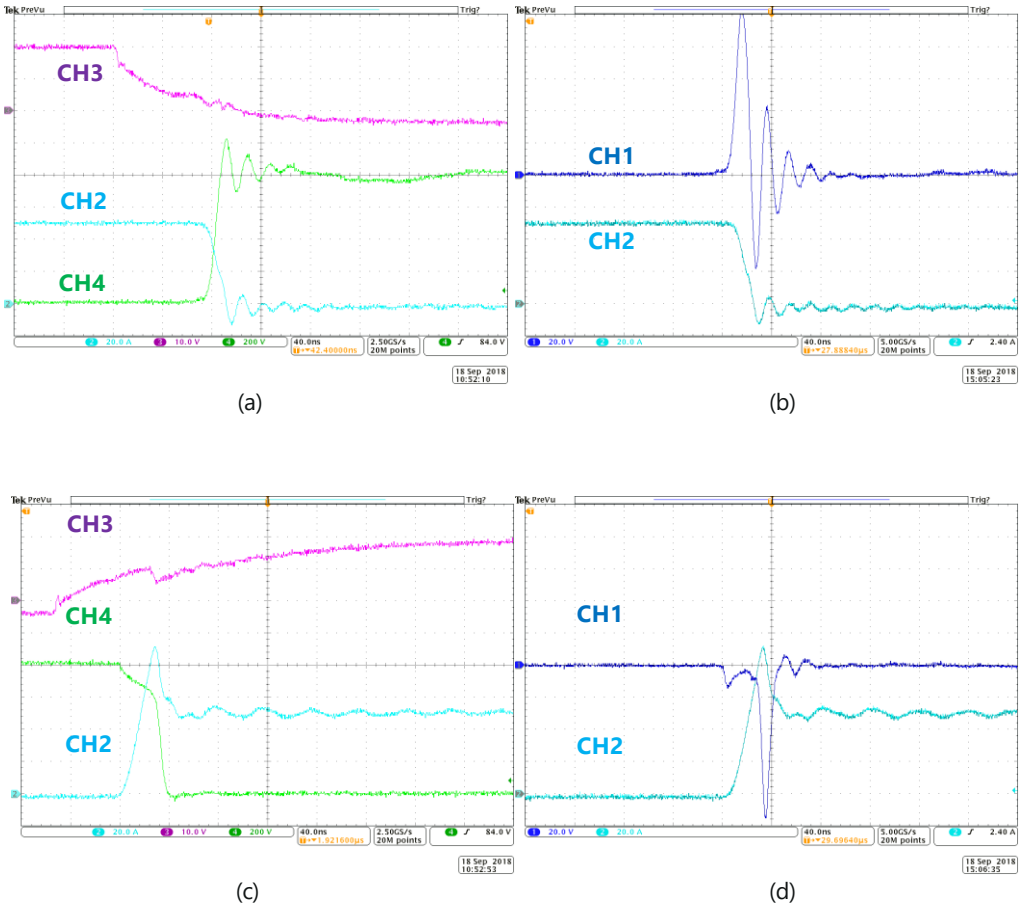


Figure 2. UF3C120040K4S turn-off (a) and turn-on (c) waveforms with snubber. Snubber Rs voltage at turn-off (b), turn-on (d). CH1: Snubber Rs voltage (20V/div); CH2: Drain current (20A/div); CH3: VGS (10V/div); CH4: VDS (200V/div). (VDS 800V, ID 50A, 125°C, VGS 20V/-5V, Rgon 50Ω, Rgoff 33Ω, snubber Cs 115pF, snubber Rs 10Ω).

In Figure 2, experimental results of UF3C120040K4S double pulse tests shows the actual voltage across Rs at 50A load current. UF3C120040K4S [3][4] is a 4-lead TO-247 device with kelvin-source. It is the fastest and highest efficiency series in the UnitedSiC product portfolio. The Rs loss is integrated using I^2R over one switching cycle including turn-on and turn-off transients.

Figure 3 shows the comparison between measured Rs loss and conventional CV^2 estimation. The large difference stems from the fact that for inductive load turn-off transients the snubber Cs is not charging at constant voltage. The current flowing through Rs is defined by $Cs \cdot dV/dt$. Therefore, Rs loss is load current dependent. Higher load current leads to faster dV/dt thus more current is going through Rs.

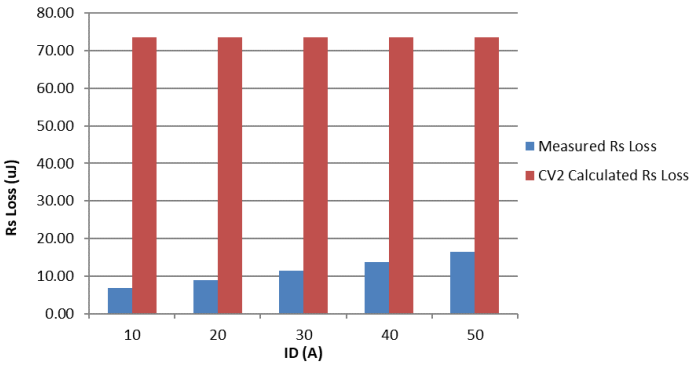


Figure 3. UF3C120040K4S snubber Rs loss measurement vs. conventional CV^2 calculation.

3. Double Pulse Test (DPT) Setup

The DPT schematic shown in Figure 1 is used to study the effect of snubber. Snubber Cs and Rs are assembled close to high side and low side devices as shown in Figure 4. The same FET is used in the high side (HS) and low side (LS) locations in a half-bridge configuration. Both HS and LS are heated to 125°C by a ceramic heater. High side VGS is always -5V with the same turn-off Rg (Rgoff) as the low side device.

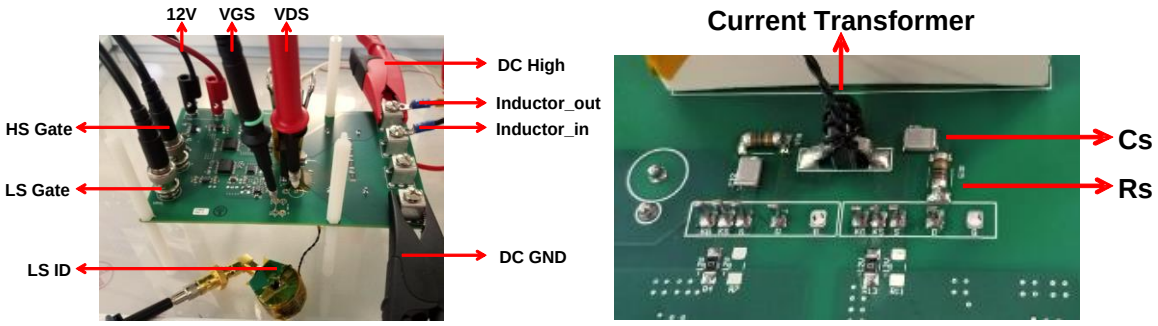


Figure 4. DPT with side-by-side snubber on both high side and low side devices.

All test waveforms are measured on the low side. The oscilloscope used for this test is Tektronix MDO4104B-6. VGS and Rs voltage is measured with Tektronix TPP1000 1GHz voltage probe. VDS is measured with Pomona 6498 400MHz voltage probe. DUT drain current is measured at the source using a 1:10 turn ratio transformer followed by a Pearson 2878 70MHz Current

transformer. The compact 10:1 transformer is constructed with a ferrite toroid (TC9.5/4.8/3.2-3E27) core as shown in Figure 4.

4. Hard Switching Effect

This section explains the benefit and trade-off of using a snubber in hard switching applications. The purpose of using side-by-side RC snubber is to reduce the voltage spike and ringing at high currents during the turn-off transition. As stated in section 2 this method has lower net losses than using SiC slowed by high Rgon/Rgoff values. Figure 5 compares turn-on loss (Eon) and turn-off loss (Eoff) of 1200V 40mΩ devices from 3 SiC manufacturers. As shown in Figure 1 the current measurement includes both the device drain current and the snubber current. Therefore, the loss value of UF3C120040K3S in Figure 5 includes snubber loss as well. Table. 1 summarizes the testing conditions.

Part Number	Package	VDS	Temp	VGS	Rgon/Rgoff	Rs	Cs	Cd
UF3C120040K3S	TO-247-3L	800V	125°C	20/-5V	5/33Ω	5Ω	330pF	0.1uF
UF3C120040K4S	TO-247-4L	800V	125°C	20/-5V	50/33Ω	10Ω	115pF	0.1uF
Competitor A	TO-247-3L	800V	125°C	20/-5V	10/10Ω	X	X	0.1uF
Competitor B	TO-247-3L	800V	125°C	20/-5V	10/10Ω	X	X	0.1uF

Table 1. DPT conditions for 4 SiC FET devices. "X" means there is no snubber.

Figure 5 shows that for TO-247-3L (3 lead) using snubber with fast switching device has lower switching loss from medium to high load. UF3C120040K4S (TO247-4L) has the lowest switching loss because it is a 4-lead kelvin device. It also uses lower snubber Cs value.

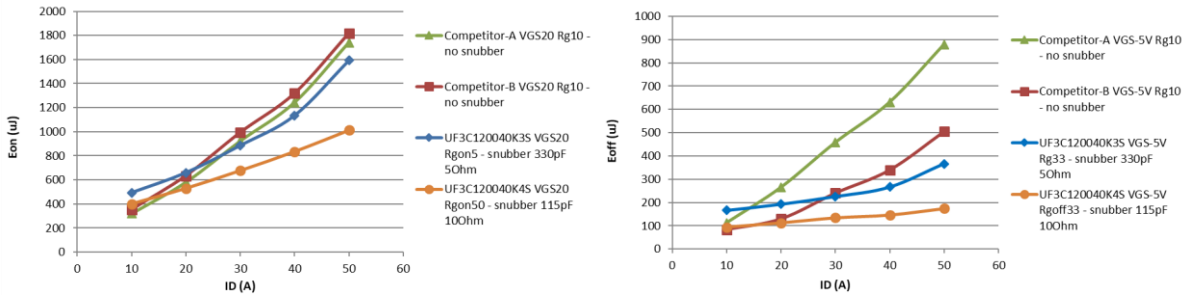
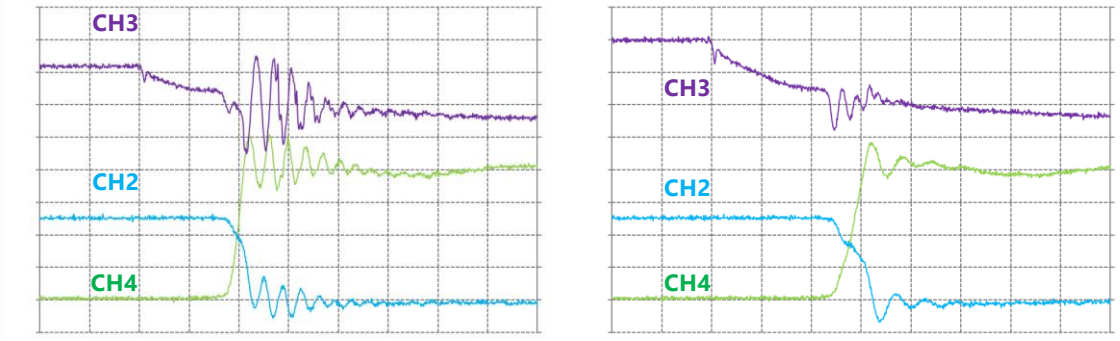


Figure 5. Hard switching Eon Eoff comparison among 1200V 40mΩ SiC devices at VDS 800V, VGS -5V.

Figure 6 shows the improvement of V_{DS} and V_{GS} waveform of the fast switching SiC device (UF3C120040K3S TO247-3L) at turn-off with and without the RC snubber. The V_{DS} spike and ringing is greatly reduced. CH1 shows the voltage across snubber Rs on the low side device.



(a) (b)

Figure 6. UF3C120040K3S turn-off without snubber (a), with snubber (b) at VDS 800V, ID 50A, VGS -5V, Rgoff 33Ω. CH2: Drain current (20A/div); CH3: VGS (10V/div); CH4: VDS (200V/div).

Therefore, using a fast SiC device like the UF3C series with a snubber can reduce overall loss at full load without introducing excessive voltage overshoot and ringing. The tradeoff is that snubber loss lowers light load efficiency.

5. Soft Switching Effect

For soft switching applications, zero-voltage switching at turn-on during normal operation makes Eon negligible compared to Eoff loss. The turn-off loss for soft switching is different from hard switching. In hard switching part of the turn-off loss energy is stored in Coss and Cs. This energy is then dissipated in device channel during the next turn-on transient. However, in soft switching this energy is recycled and transferred to load. Therefore, the actual turn-off loss for soft switching should exclude the Coss and Cs energy from hard switching turn-off loss measurement. Figure 7 compares actual turn-off loss (Eoff) of 1200V 40mΩ devices from 3 SiC manufacturers. Coss energy is referred to as Eoss. Cs energy is referred to as Ecs. To fully recycle the energy in Cs, the Rs for soft switching should be positioned with the power loop decoupling capacitor Cd as shown in Figure 1b.

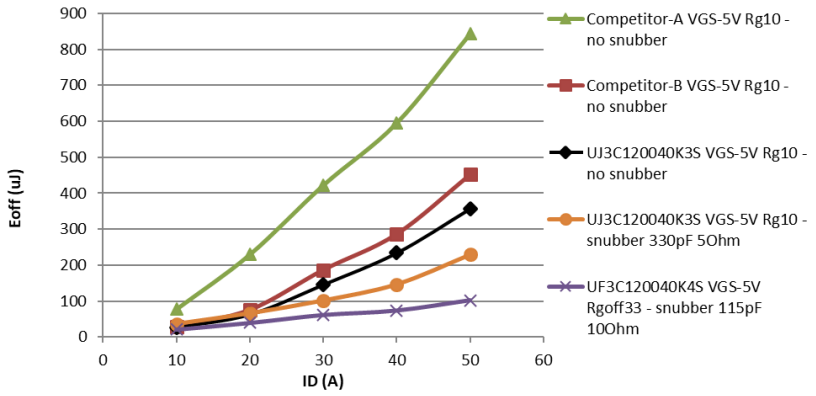


Figure 7. Soft switching Eoff comparison among 1200V 40mΩ SiC devices at VDS 800V, VGS -5V. Soft switching Eoff is calculated as (DPT measured Eoff) minus (Eoss + Ecs).

The black and yellow curve in Figure 7 also shows that adding snubber Cs to a half bridge will reduce soft switching turn-off loss. This is because for inductive loads the turn-off dV/dt diverts current to charge the DUT Cs, and discharge the HS Cs, diverting current from the DUT channel, and reducing the Eoff. Adding a snubber Cs also helps designers match the circuit performance better when multiple power device suppliers are present. The tradeoff is that adding Cs would require higher minimum energy to maintain ZVS at light load.

6. Conclusion

Switching fast SiC FETs in standard TO packages requires users to either slow the FETs down, or use a RC snubber to reduce voltage overshoots and ringing. We have shown here that snubber Rs loss is much lower than the conventional $f \cdot CV^2$ estimate. We have further demonstrated that very small values of snubber capacitors can help manage the voltage overshoots, given the low Coss values of UnitedSiC FETs. This leads to snubber losses small enough to allow regular surface mount components to be used, even when switching 50A, 800V per FET. Using UnitedSiC fast devices (UF3C series) with an RC snubber enables a better trade-off in minimizing switching loss while managing turn-off voltage spikes and ringing, and is decidedly superior to just slowing devices with external gate resistors.

References

[1] Maxim Integrated, "Correct Snubber Power Loss Estimate Saves the Day". [Online]. Design Solutions Power. Available: https://www.maximintegrated.com/content/dam/files/design/technical-documents/design-solutions/DS32-Correct-Snubber-Power-Loss-Estimate-Saves-the-Day.pdf

[2] Link to UnitedSiC cascode user guide: https://unitedsic.com/wp-content/uploads/2018/10/UnitedSiC-SiC-FET-User-Guide-Q4-2018_V4.pdf

[3] Link to UnitedSiC datasheet: https://unitedsic.com/cascodes/

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