SiC in Solar Inverter Topologies

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1 Introduction

The design of a renewable energy inverter involves many tradeoffs, including cost, electrical specifications, efficiency, features, reliability, installation cost, etc. Adding to these assorted considerations is the radically improved performance of SiC versus silicon-based semiconductors and their cost differences, which makes evaluating various topology options like comparing apples to oranges and pears. Models for efficiency, cost, and reliability are needed to optimize tradeoffs and to dependably predict their overall effects. This note focuses on semiconductor power loss estimations to model efficiency of solar inverters utilizing UnitedSiC cascodes and diodes in three-level versus two-level topologies with an input booster. What we are trying to answer here is when to use which topology.

2 Solar Power Generation System

Commercial and utility scale solar systems are compelled by maximizing profit from selling electrical energy. This places a strong emphasis on system efficiency; maximizing the electrical power generated while minimizing interconnection and conversion losses. In the simplified block diagram of Figure 1, a grid-tied commercial solar system comprises a large solar panel array connected in series-parallel through combiner boxes to a central inverter, which is in turn connected to the AC power grid. The inverter may include an input DC-DC converter (a booster for example), enabling a wide input voltage range from the panel array while maximizing inverter efficiency, as well as the option to interconnect other power sources or energy storage.

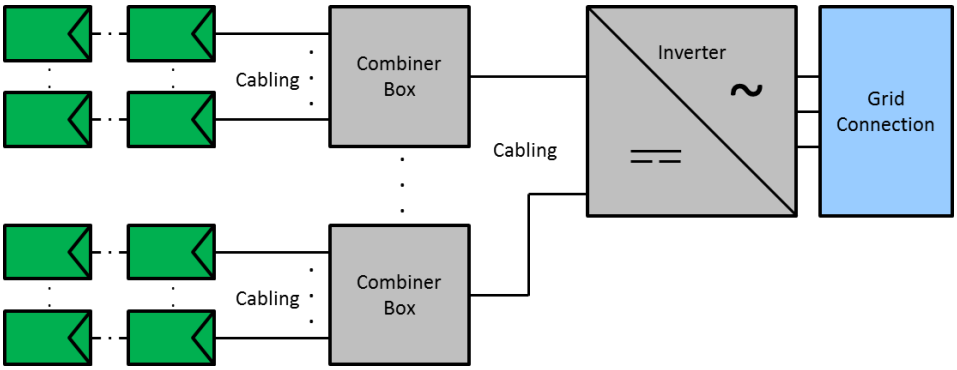


Figure 1 Solar power generation block diagram

The panel array is often oversized, with its power output capacity exceeding the power rating of the inverter during ideal insolation conditions. This maximizes the energy harvest by operating the inverter at full rated power during a range of common insolation conditions. The reliability model for designing the power converters must include temperature swings between cool nighttime with no power processing, and daylight operation at full power with sun loading adding to the heat inside the weatherproof cabinet. This is especially important considering that many solar inverter failures are due to overheated control electronics rather than burned out power semiconductors. Minimizing heat dissipation is therefore another motivation for maximizing efficiency. Imagine a 100 kVA inverter operating at 95 % efficiency. Approximately 5 kW of heat must be removed from inside the inverter cabinet, roughly the amount of heat output from five small space heaters running at full power. Increasing the efficiency by 3 % is tantamount to turning off three space heaters inside the cabinet, a huge benefit!

Cabling and interconnect power loss become increasingly significant as power converter efficiency improves. Cost savings in cabling and power converters are achieved by operating at higher DC voltage.

3 Topology Selection

Let us consider as an example a 50 kVA inverter capable of any power factor from zero leading to zero lagging (unidirectional power flow), but with full rated power output at unity power factor. For this example galvanic isolation between DC source and a 480 VAC 3-phase grid connection is not required. The solar panel array can be configured for 1000 V maximum.

For the three-phase inverter itself, the common topology options are shown below in Figure 2 and designated as:

- Two-level (conventional six-pack)
- Transistor clamped three-level (TNPC)
- Diode neutral point clamped three-level (NPC)

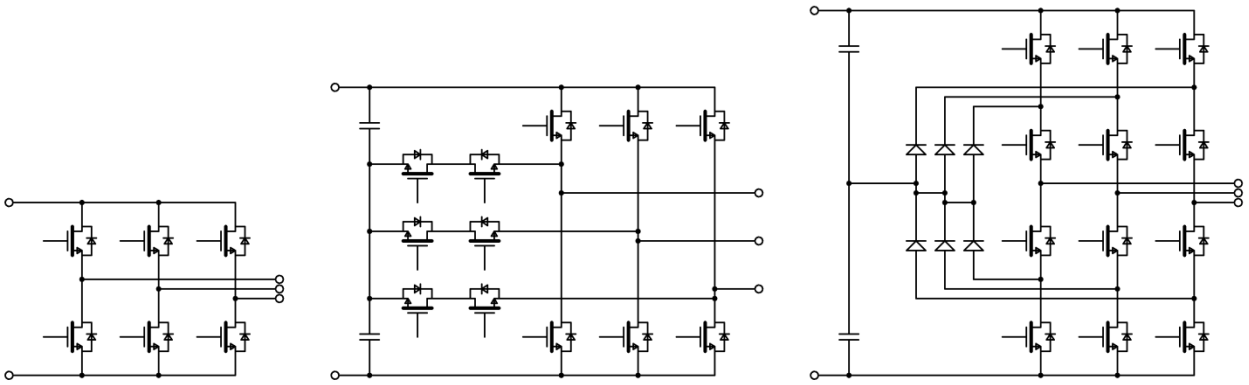


Figure 2 Inverter topologies (a) two-level, (b) transistor clamped TNPC, (c) diode neutral point clamped NPC

Added to these is the option to include a two-level or three-level booster at the input, with an example of each shown in Figure 3. The booster diode and switch functions alternate between devices depending on power flow direction. (The circuit alternates between boost or buck mode.) This demands good reverse conduction and recovery characteristics of the power devices, an area where UnitedSiC cascodes excel.

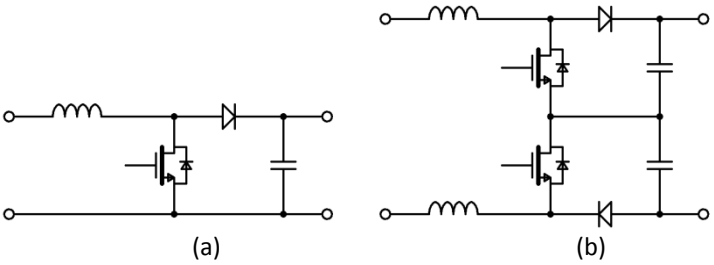


Figure 3 Conventional booster (a), and three-level booster (b)

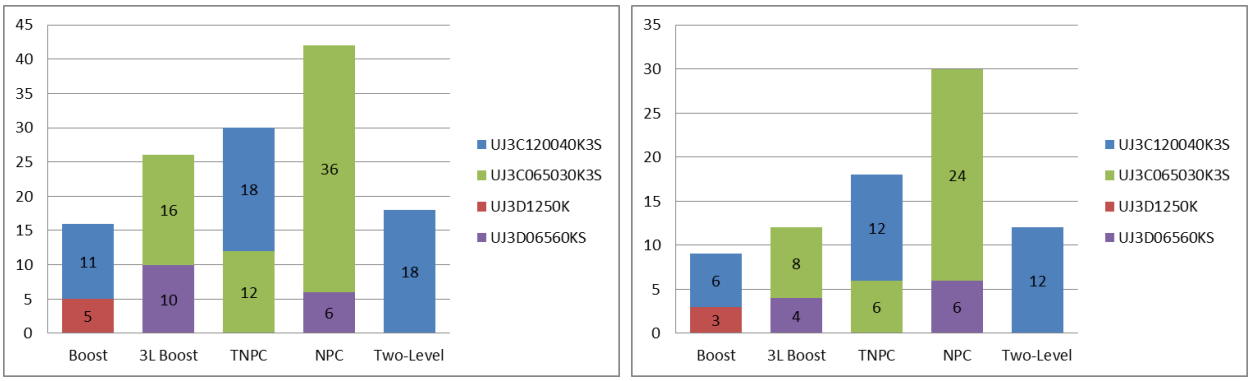
The criteria for determining the number of parallel semiconductor devices in each switch position to reach the 50 kVA specification is that the junction temperature should remain 25 °C below the maximum rated junction temperature, at unity power factor and otherwise worst-case conditions. The reliability and cost models might mandate a different temperature margin, but in any case, estimating junction temperature with a power loss model is a good way to determine how many parts to parallel [1].

There is no mention of a requirement for electrical isolation of the heat sinks in the specifications for this design example. Isolation material between the device package and heatsink greatly increases the thermal resistance from package case to heatsink, which in turn increases the number and/or size of devices required to meet the output power requirement. With SiC devices it may be advantageous to use non-isolated, fan-cooled heat sinks

inside an enclosure that prevents contact with high voltages. On the other hand, it may be convenient to use the enclosure itself as a heatsink, in which case electrical isolation is required. Both situations are covered in this example by assuming a case-to-heatsink thermal resistance of 2.0 or 0.35 °C/W for isolation material or thermal grease respectively between the package case and the heatsink. The heat sink temperature is assumed to be 100 °C (air cooled).

An input booster is required for 1000 VDC maximum input with a 480 VAC grid connection, otherwise the panel voltage range would be too narrow to be usable (only about 25 % swing between ~800 and 1000 V). Let the booster regulate voltage to the inverter at 800 V. If the panel voltage exceeds that (actually a hysteresis window), the booster stops switching and allows current to simply pass through. With the booster, the panel voltage range can be very wide. For example, a 5-to-1 boost ratio puts the minimum panel voltage at 170 V. We will use a more conservative 300 V minimum panel voltage for this design.

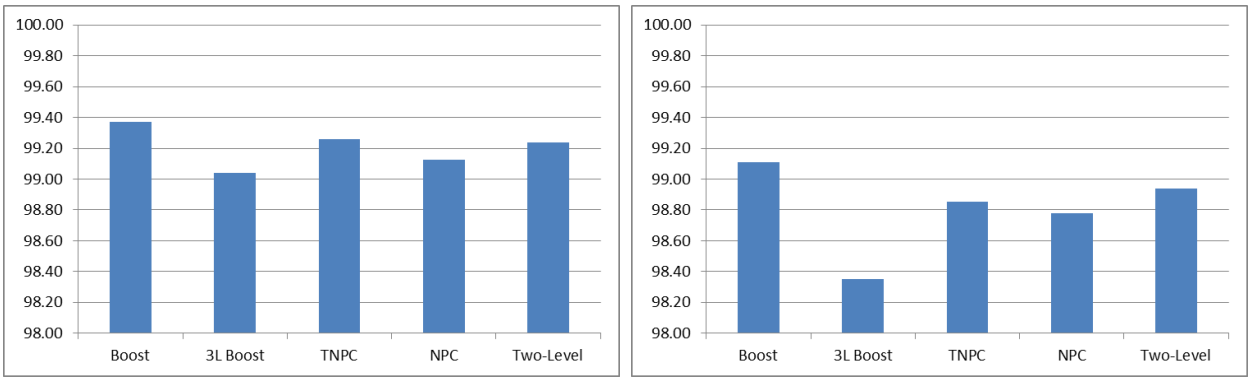
The power semiconductors considered include UJ3C120040K3S, UJ3C065030K3S, UJ3D1250K, and UJ3D065060KS from United Silicon Carbide. The switching frequency is set at 25 kHz. These SiC devices could certainly switch faster than this. A separate study could be made to optimize switching frequency versus other competing tradeoffs, but this is a reasonable operating frequency at these voltages. The power loss model results [2, 3] are shown below in Figure 4 and Figure 5, with 300 to 800 V boost (worst case), and 800 V input to the inverters.



(a) (b)

Figure 4 Total device count (a) with isolation material, $R_{\theta CS}$ = 2.0 °C/W, (b) non-isolated heatsinks, $R_{\theta CS}$ = 0.35 °C/W

Eliminating isolation of the heatsinks results in a 29 to 54 % reduction in the number of parallel devices required. To keep things simple, only large capacity cascodes and diodes were considered. Further cost savings could be achieved especially for non-isolated heatsinks by considering smaller devices. The large device count of the NPC inverter topology stands out, but there is a distinct advantage to this topology, which will be discussed.



(a) (b)

Figure 5 Semiconductor efficiency (a) with isolation material, $R_{\theta CS}$ = 2.0 °C/W, (b) non-isolated heatsinks, $R_{\theta CS}$ = 0.35 °C/W

The semiconductor efficiency with non-isolated heatsinks is generally lower due to fewer parts in parallel and consequently higher combined on-resistance. The efficiency of the conventional booster is noticeably better than the three-level booster, at least at 25 kHz. Increasing the switching frequency causes switching loss to far surpass conduction loss in the conventional booster, until eventually the three-level booster is more attractive. Staying with our 25 kHz example, the conventional booster wins.

Among the inverter topologies, conventional two-level is the apparent winner both in device count and efficiency. But lurking in the scant specifications for this design example is the fact that galvanic isolation between DC input and AC output is not required. The problem is that a three-phase, two-level inverter has high common-mode voltages between its DC input and AC outputs, which is unacceptable in a transformer-less installation. Adding a line-frequency transformer adds considerable cost and weight. A fourth inverter leg could be added, an isolated booster could be used, or a three-level inverter could be used. A three-level inverter can be modulated in such a way (by using medium vectors on a state map) to eliminate, or at least vastly reduce the common mode voltage swings. This has cost, efficiency, and simplicity advantages over an isolated DC-DC converter. The drawback is reduced DC voltage utilization, but that is workable with a front-end booster. The DC link voltage would need to increase by at least 13 % (and power loss calculations double checked) compared to the minimum required for nearest vector PWM. The harmonics are similar to a two-level inverter, but this is not a major concern considering the increased switching frequency allowed by SiC devices compared to IGBTs; the output filter would still be much smaller.

The TNPC is the clear winner over NPC for both part count and efficiency, again at the modest 25 kHz switching frequency. We could stop here and say that our inverter system looks something like the one shown below.

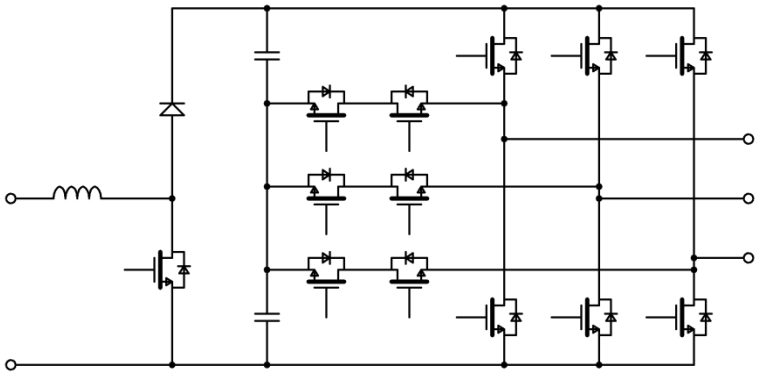


Figure 6 Booster paired with TNPC inverter

In reality, with all the parallel parts required, it only makes sense to divide the circuitry. For example, the non-isolated heatsink booster could be built as three boosters, each with two parallel cascodes and a single diode. The inverter could be divided in a similar manner, possibly into two or some other number of parallel inverters. An obvious advantage of multiple boosters is it supports multiple panel strings, increasing flexibility when installing the solar panel array. Another advantage is interleaving the switching to reduce ripple currents and electrical noise, if there is sufficient digital processing power in the control system. A third advantage is low power efficiency can be improved by shutting down gate drive circuitry for unused channels.

There is a possible disappointment with this design. Long-term operation at 1000 V with 1200 V rated devices could result in excessive cosmic radiation failures (single event burnout). Even SiC devices are susceptible, and similar to silicon-based device, should have at least 25 % voltage margin, preferably more, for long-life applications such as solar inverters. The voltage margin at 900 V operation is 25 %. Whether this design is acceptable depends a reliability model that factors in SEB [4].

Suppose the reliability model requires more voltage margin, or suppose the requirement is to operate with up to 1500 V DC input. A three-level booster and the NPC inverter topology would then be the winners. This highlights the real strength of the NPC inverter topology in particular – it enables high voltage operation.

4 Implementation Details

Connecting the clamp transistors common-drain as in the TNPC inverters shown in Figure 2(b) and Figure 6 has the advantage of reducing the required number isolated power supplies from six to four compared to connecting them common-source. The layout is different for common-source versus common-drain connection when taking advantage of the backside drain connection of a TO-247 package, as in the non-isolated heatsink case (or of a chip in a power module).

In a three-level inverter, two switches commonly remain static with one off and the other on for half a line cycle. Holdup time must accommodate this if bootstrap gate drive power is used. The UJ3C series cascodes can be held on with 10 V or even a little less. For fast turn-on switching speed, 15 to 18 V gate drive voltage is recommended. Negative gate drive voltage is optional, with -5 V being ideal.

By changing the diodes in the boosters to cascodes, the booster-plus-inverter can process power in two directions, meaning it can act as a DC-to-AC inverter, or as an AC-to-DC active front end rectifier, which is often required for energy storage and uninterruptible power supply applications. In this configuration, the function of the cascodes alternates between switch and diode depending on the direction of power flow. Heat loading changes between inverter and rectifier modes, so device count would need to be equal for each switch position in the booster; eleven or six for isolated versus non-isolated heatsinks respectively for this example design.

5 Summary

When choosing a booster topology, the switching frequency and voltages matter. For inverters using SiC, both TNPC and NPC have a slight switching frequency advantage over conventional two-level inverters. The three-level inverters have the huge advantage of mostly eliminating common-mode voltage swings (depends on modulation strategy). The switching frequency advantage of NPC over TNPC is so slight with SiC devices that TNPC should be used when possible, and NPC should be used when high operating voltage demands it.

6 References

[1] M. Schweitzer, I. Lizama, T. Friedli, J. Kolar; “Comparison of the Chip Area Usage of 2-level and 3-level Voltage Source Converter Topologies”, IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society
[2] I. Staudt; “3L NPC & TNPC Topology”, Semikron Application Note AN-11001, 2015-10-12
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[4] C. Davidson, E. Blackmore, J. Hess; “Failures of Terrestrial MOSFETs Due to Single Event Burnout,” International Telecommunications Energy Conference, September 2004, pp. 503-507