

## UnitedSiC JFET in Active Mode Applications

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Active mode

### 1 Introduction

Power MOS devices, which include power MOSFETs of various construction materials and gate structures, as well as JFETs and IGBTs are three-terminal devices with current flow controlled by the gate. In most power electronic applications, the gate is driven to either block current flow with the device fully off; or fully on with minimal conduction loss. The transition between the on and off states generates high heat, and so the transition time is kept as short as practical to minimize switching power loss. Such is the art of hard-switched switch mode power supply (SMPS) design.

There are many applications where the switching transition is unavoidably proportionate to the on and off switch states, or where the operating point is deliberately set within the transition region. This application note addresses operation of both power MOS and UnitedSiC JFETs in these applications.

### 2 Operating Region Definitions

The output characteristic of a power MOS or JFET has three regions, cutoff, active, and ohmic, as shown for a UnitedSiC JFET in Figure 1. In cutoff, the device is considered to be off since only very small current flows. When the gate-source voltage is driven sufficiently high, the device enters the ohmic region, where the drain-source voltage  $v_{DS}$  is small and current flow is largely determined by on-resistance.

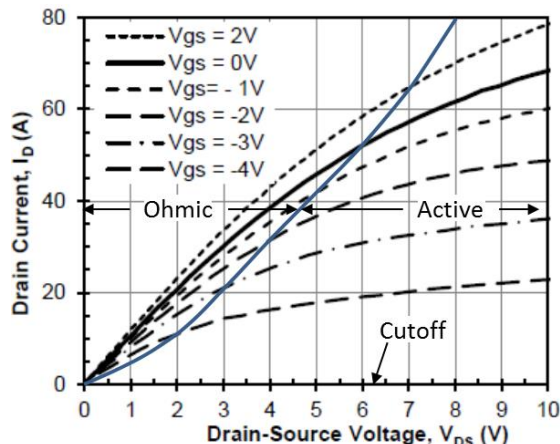


Figure 1 Output characteristic of a 1200 V UnitedSiC JFET at 125 °C

The boundary of the ohmic region is defined by:

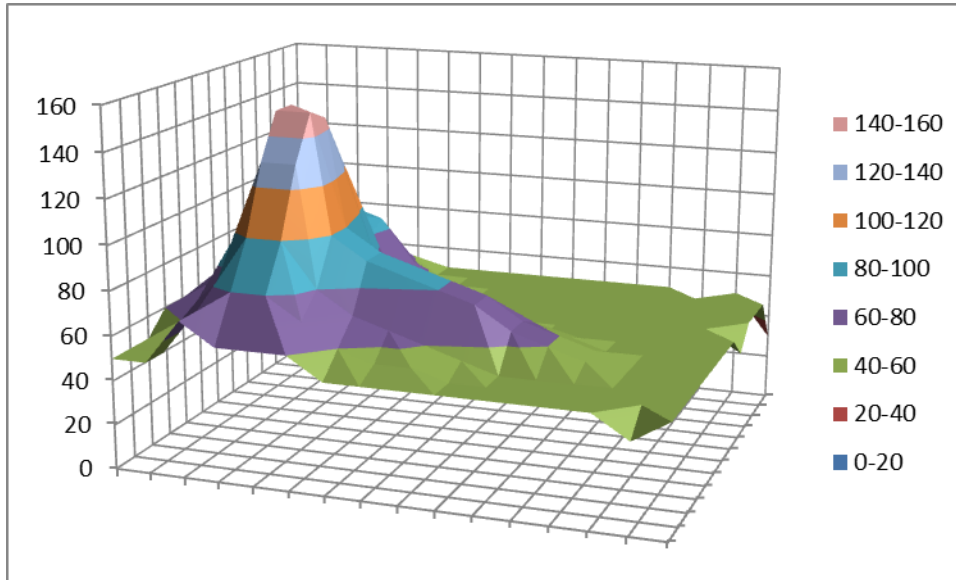
$$v_{GS} - V_{GS(th)} > v_{DS} > 0 \quad (1)$$

Between the ohmic and cutoff regions is the active region, designated as such to avoid confusion between different meanings for linear and saturation regions for power MOS, JFET, and bipolar transistors. Operation within the active region is therefore designated active mode in this application note, even though in much literature it is called linear mode. Drain current in active mode depends mostly on gate-source voltage, although especially at low  $v_{DS}$  a dependence on drain-source voltage is clearly seen in Figure 1 as well.

The simultaneous current and voltage supported by a device in active mode result in high power that must be dissipated as heat. Economic functioning in active mode therefore requires full utilization of the forward safe operating area (FSOA), and understanding device limitations is vital to achieve reliable operation.

### 3 Root Cause of Power MOS Failures in Active Mode

Applications operating in active mode are arguably the most plagued by failures in spite of operating well within the power MOS datasheet FSOA. The cause of failures is thermal instability, which results in hot spots from current focusing.



**Figure 2 Representation of 5x5 mm power MOS temperature distribution (°C) in [1] clearly showing hot spot phenomenon**

Inevitable temperature gradients across a power device chip can lead to hot spots because of a positive change in current with increasing temperature. A hotter area on the chip focuses more current that causes further heating and possibly failure from thermal runaway in a localized area. In [1] the effect of thermal instability was shown graphically by measuring temperatures across a power MOS in active mode. The results are roughly reproduced in Figure 2, clearly showing a hot spot with a large difference between minimum, maximum, and average temperatures. The current crowding and the temperature in the hot spot can be very high, resulting in a burn-out spot and device failure.

In switch-mode applications current crowding is usually not an issue; the active region is traversed very quickly, and current in the ohmic region of operation is limited by channel and bulk resistances with their corresponding strong positive temperature dependence. Active mode operation however results in high power dissipation for a thermally significant length of time. Therefore, thermal instability limits the true safe operating area of a power device in active mode. Fortunately, many power MOS manufacturers are aware of this and now publish FSOA curves with a reduction from constant power dissipation lines in the high voltage side of the FSOA. This application note takes this a step further, and based on the work in [1-3], the actual onset of thermal instability is estimated based on published datasheet information.

### 4 Analysis of Thermal Instability of Power MOS in Active Mode

Thermal instability occurs when the electrical power increases more than can be thermally dissipated [4]. With electrical and thermal power denoted as  $P_G$  and  $P_\theta$  respectively, thermal stability is mathematically expressed as:

$$\frac{\partial P_G}{\partial T} \leq \frac{\partial P_\theta}{\partial T} \quad (2)$$

With  $\partial T = \partial P_{\theta} \cdot Z_{\theta}$  and  $\partial P_G = \partial i_D \cdot v_{DS}$ , where  $Z_{\theta}$  is the thermal impedance (time-dependent thermal resistance), the condition of thermal stability can be expressed as:

$$v_{DS} \cdot \frac{\partial i_D}{\partial T} \leq \frac{1}{Z_{\theta}} \quad (3)$$

Power MOS drain current in the active region can be approximated as:

$$i_D = K_{MOS} \cdot (v_{GS} - V_{GS(th)})^2 \quad (4)$$

In equation (4),  $K_{MOS} = \mu_n \cdot C_{ox} \cdot \frac{W}{2 \cdot L}$  where  $\mu_n$  is the inversion layer majority-carrier mobility,  $C_{ox}$  is the gate oxide capacitance per unit area,  $W$  is the gate width, and  $L$  is the channel length. The capacitance  $C_{ox}$  is determined by the dielectric constant of the gate insulator and its thickness. It is therefore constant, as are gate width  $W$  and channel length  $L$ . The electron mobility  $\mu_n$ , and hence the magnitude of  $K_{MOS}$ , decreases with increasing temperature and drain current  $i_D$ .

At sufficient drain current, the current limiting effect from decreased electron mobility exceeds any increase in current from the temperature-dependent threshold voltage. It is therefore possible to roughly predict operating conditions that are thermally stable for a power MOS based on the stability criterion that the drain current must not increase with temperature. As a first-order approximation [1, 2], differentiate equation (4) with respect to temperature. The result is the drain current temperature coefficient (DCTC), denoted as  $\alpha_T(i_D)$  as a function of drain current. A power MOS is always thermally stable if the DCTC is less than or equal to zero.

$$\frac{\partial i_D}{\partial T} = \alpha_T(i_D) = \frac{\partial K_{MOS}}{\partial T} \cdot \frac{i_D}{K_{MOS}} - 2\sqrt{K_{MOS} \cdot i_D} \frac{\partial V_{GS(th)}}{\partial T} \leq 0 \quad (5)$$

For power MOS,  $\frac{\partial K_{MOS}}{\partial T}$  is always negative, and therefore thermal instability is directly caused by the  $-2\sqrt{K_{MOS} \cdot i_D} \frac{\partial V_{GS(th)}}{\partial T}$  term, and specifically by  $\frac{\partial V_{GS(th)}}{\partial T}$ , which is the threshold voltage temperature coefficient (TVTC). It follows then that a device is always thermally stable in active mode if its TVTC is greater than or equal to zero.

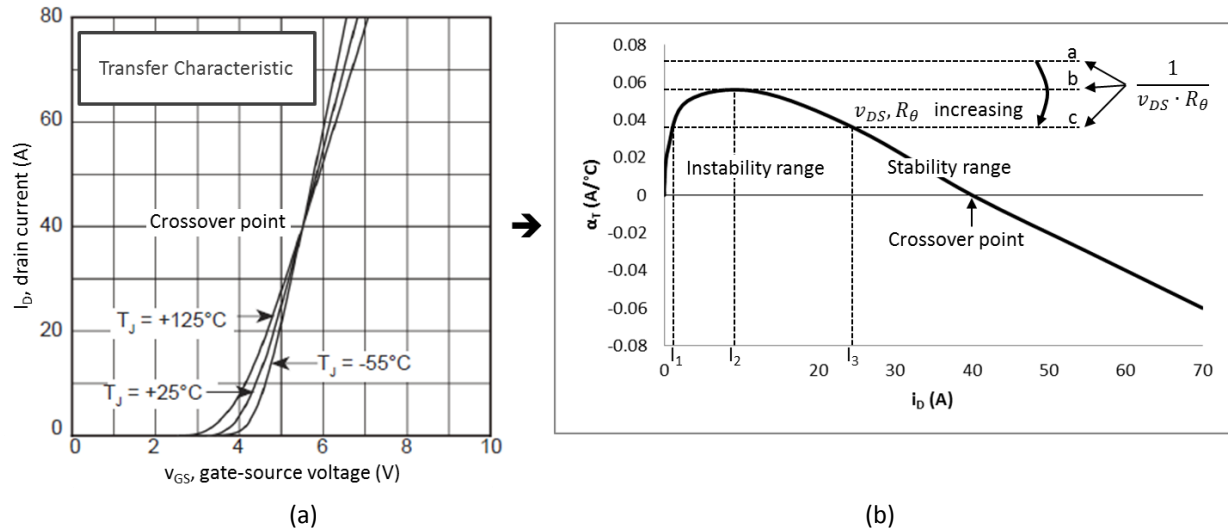
A stability factor  $\gamma$  is introduced by substituting in  $\alpha_T(i_D)$  in equation (3) and rearranging (in [1-3] it is called an instability factor  $S$ ):

$$\gamma = \alpha_T(i_D) \cdot v_{DS} \cdot Z_{\theta} \leq 1 \quad (6)$$

Rewriting equation (6) results in a useful stability criterion:

$$\alpha_T(i_D) \leq \frac{1}{v_{DS} \cdot Z_{\theta}} \quad (7)$$

The challenge now is determining DCTC curve  $\alpha_T(i_D)$ . It can be calculated from device design parameters, but these are usually not published; or it can be measured. Fortunately, the transfer characteristic (derived from output characteristic data) is published in most datasheets and contains the needed DCTC data.



**Figure 3 Power MOS (a) transfer characteristic (b)  $\alpha_T$  versus  $i_D$  derived from transfer characteristic**

The information in the transfer characteristic can be transposed to a graph of  $\alpha_T$  versus current, with each data point at a given gate-source voltage, as shown in Figure 3(b) by subtracting the current at 125 °C from that at 25 °C, and then dividing by 125 – 25 = 100. Such a graph is very useful for estimating the onset of thermal instability as well as for comparing the inherent stability of different power devices.

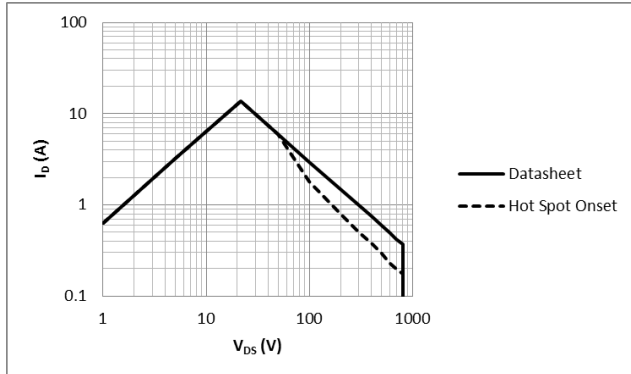
Consider the steady-state case (non-pulsed), so that  $Z_\theta$  becomes simply  $R_{\theta JC}$ , for which the published value of junction-case thermal resistance from the datasheet is used. Using the datasheet  $R_{\theta JC}$  value introduces some variability due to different margin between power MOS manufacturers, and using the maximum value from the datasheet naturally results in a worst case analysis. It yields however a reasonable approximation that provides significant insight into power MOS thermal stability based on published datasheet information. Equation (7) is evaluated for various values of  $v_{DS}$  as follows. In Figure 3(b), line ‘a’ indicates a value of  $\frac{1}{v_{DS} \cdot R_{\theta JC}}$  that is always greater than the  $\alpha_T(i_D)$  curve, and so the power MOS is always thermally stable at this low drain-source voltage, even when operating below the current crossover point in Figure 3(a). Line ‘b’ intersects the peak of the  $\alpha_T(i_D)$  curve, thus indicating the drain-source voltage at which hot spots can begin to form. Line ‘c’ intersects the  $\alpha_T(i_D)$  curve in two places, indicating a thermal instability range. Below  $I_1$  the power dissipation is low enough that current crowding is insignificant. If the current exceeds  $I_2$ , then a hot spot will form, and  $I_3$  is the peak current that is subsequently reached in the hot spot, although the device could fail first.

Extending the analysis to the FSOA, the onset of thermal instability can be plotted by calculating the maximum power dissipation based on thermal impedance and junction and case temperatures, at various drain-source voltages. Then at the same drain-source voltage points, calculate  $\frac{1}{v_{DS} \cdot R_\theta}$  values. Finally, reduce the drain current (power dissipation) if necessary, such that each adjusted  $\frac{1}{v_{DS} \cdot R_\theta}$  value is above or equal to the  $\alpha_T(i_D)$  curve. Each point where the current was reduced roughly indicates the onset of thermal instability.

The current values along the horizontal axis of the  $\alpha_T(i_D)$  graph are important for FSOA analysis. The curve in Figure 3(b) was made from data points corresponding to where two temperature curves, 25 and 125 °C in this case, have the same gate-source voltage. The current values for the horizontal axis of the  $\alpha_T(i_D)$  graph can be interpolated as the average currents from the 25 and 125 °C data sets from Figure 3(a).

An example FSOA analysis is shown in Figure 4 for an 800 V, 0.75  $\Omega$  conventional MOSFET. Clearly the predicted onset of thermal instability is far below the datasheet FSOA boundary at voltages above about 50 V. In this example the case temperature is held at 25 °C, which is also unrealistic. Important information can be gleaned

from it nonetheless because it gives a rough indication of maximum safe power dissipation versus voltage, regardless of case temperature.



**Figure 4 DC FSOA and estimated thermal stability boundary with  $T_J = T_{Jmax}$  and  $T_C = 25\text{ }^\circ\text{C}$  for an 800V silicon MOSFET**

Plotting an FSOA graph at different case and junction temperatures is straightforward. Current at the low voltage side is limited by  $R_{DS(on)}$  instead of power dissipation. The peak current is at maximum power dissipation, calculated as  $I_{peak} = \sqrt{\frac{P_{D,max}}{R_{DS(on)}}}$ , where  $P_{D,max} = \frac{T_J - T_C}{R_{\theta JC}}$ . Beyond the peak the current is simply  $\frac{P_{D,max}}{V_{DS}}$ , until the current must be reduced at increasing voltages to prevent the  $\alpha_{T,max}(i_D) = \frac{1}{v_{DS} \cdot R_{\theta JC}}$  curve from crossing under the  $\alpha_T(i_D)$  curve as discussed above. When analyzing with respect to pulsed power, simply replace  $R_{\theta JC}$  with  $Z_{\theta JC}$  from the single pulse transient thermal impedance graph at the corresponding pulse duration. Reducing the thermal impedance shifts the  $\alpha_{T,max}(i_D)$  curve up, along with the thermal stability curve in the FSOA graph, thus reducing or even eliminating the thermal instability operating area. This is why some MOSFET manufacturers do not publish a DC FSOA curve; they only publish pulsed FSOA curves.

Reducing the peak DCTC, or equivalently reducing the magnitude of the negative TVTC increases the operating ranges of thermal stability. Also, recall from equation (5) that the device is unconditionally stable for all negative values of  $\alpha_T(i_D)$ . Specialized linear MOSFETs have reduced peak DCTC and improved FSOA. They still however exhibit thermal instability over a certain range of operating voltage, current, and temperature because the TVTC can never be reduced to zero in a power MOS. In a JFET, the TVTC can be made zero.

## 5 UnitedSiC JFET Thermal Stability and Improved FSOA

Drain current in a JFET can be roughly approximated as  $i_D = I_{DSS} \cdot \left(1 - \frac{v_{GS}}{V_{GS(th)}}\right)^2$ , which can be written in the same form as the power MOS equation (4):

$$i_D = K_{JFET} \cdot (v_{GS} - V_{GS(th)})^2 \quad (8)$$

The drain current in some JFETs actually has a significant dependence on drain-source voltage in active mode. Equation (8) is however sufficient to demonstrate thermal stability by considering that even if  $K_{JFET}$  increases with  $v_{DS}$ , it always decreases with temperature as does  $K_{MOS}$  in equation (4). JFETs are therefore always thermally stable if the TVTC is zero, which is the same criterion as for a MOSFET. UnitedSiC manufactures SiC JFETs with two types of gate structures. One has zero TVTC, and the other has a low TVTC. Both types are very well suited for active mode operation. The difference in DCTC between UnitedSiC JFETs and various power MOS devices is graphically indicated in Figure 5 below.

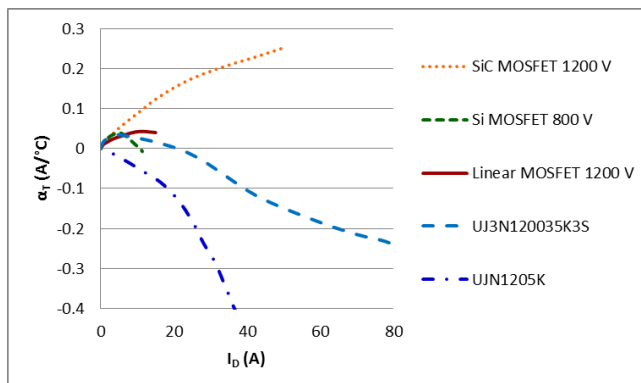


Figure 5  $\alpha_T(I_D)$  versus drain current for various device types

The peak of the DCTC is an indicator of the inherent thermal stability of a device, useful for a rough but incomplete comparison between device types. In Figure 5, it is clear the UnitedSiC 1200 V SiC JFET UJN1205K is always thermally stable because its DCTC is always negative. Next up is the UnitedSiC UJ3N120035K3S, also a 1200 V SiC JFET. It has a slightly negative TVTC and hence a positive peak in its DCTC. According to Figure 5, an 800 V conventional MOSFET has a comparable peak DCTC as a specialized 1200 V linear MOSFET, and each has an FSOA ending at 800 V. These devices have however quite different FSOAs, as will be shown. Finally, a 1200 V SiC MOSFET with similar  $R_{DS(on)}$  to the UnitedSiC JFETs has a relatively high DCTC.

Taking a somewhat different approach from the usual fixed junction and case temperatures, Figure 6 was created by adjusting the maximum power dissipation to match that at the thermal stability boundary. In other words, when operating within the respective FSOA curves of Figure 6, each device is always thermally stable, and its maximum power dissipation is constant.

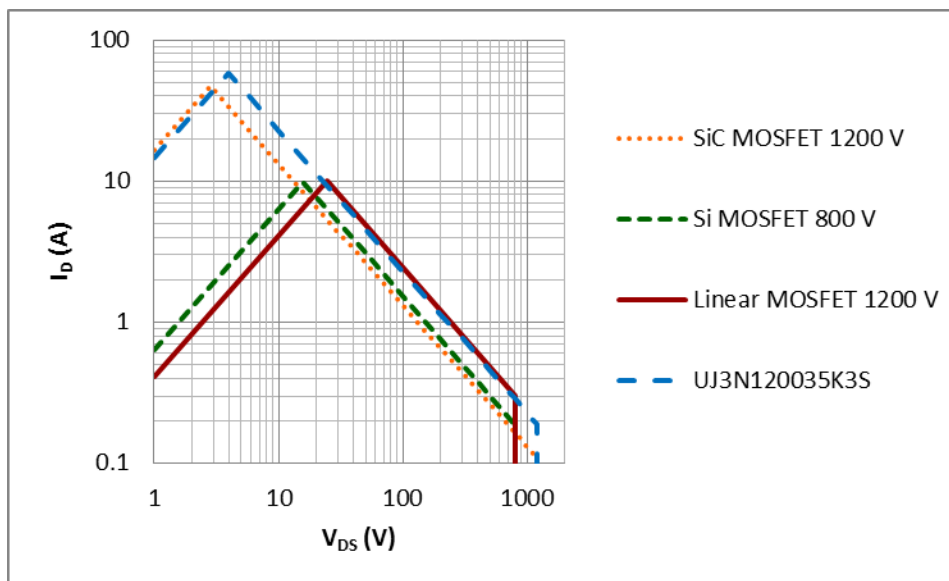


Figure 6 FSOA for various devices, within its thermal stability boundary

As expected, the SiC MOSFET has the lowest FSOA at high voltages, comparable to the conventional 800 V MOSFET. Unlike the silicon-based MOSFETs however, the SiC MOSFET and the SiC UJ3N120035K3S JFET have a huge  $R_{DS(on)}$  advantage, greatly reducing the on-voltage at correspondingly higher peak current. Both the linear MOSFET and the SiC JFET have a wide thermal stability boundary, due to the combination of low peak DCTC and thermal resistance. Only the UJ3N120035K3S JFET has significant usable FSOA above 800 V drain-source voltage,

an advantage for high voltage active mode applications. The UJN1205K was omitted from Figure 6 because it is always thermally stable, regardless of power dissipation, due to its zero TVTC. The UJN1205K is instead compared with the UJ3N120035K3S in Figure 7 below.

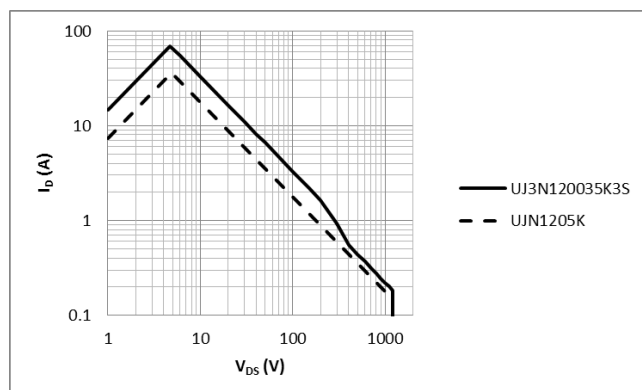


Figure 7 FSOA comparison between UnitedSiC UJ3N120035K3S and UJN1205K,  $T_J = 175\text{ }^{\circ}\text{C}$ ,  $T_C = 60\text{ }^{\circ}\text{C}$

These JFETs have very similar chip size and  $R_{DS(on)}$ , but the UJ3N120035K3S has lower  $R_{\theta JC}$  due to an improved manufacturing process. In this case the lower thermal resistance of the UJ3N120035K3S outweighs its reduction in thermal stability boundary, which limits power dissipation at or above 400 V to 220 W.

As shown above, power devices prone to thermal instability under certain conditions can operate reliably in active mode with reduced FSOA. It can be argued that SiC devices can operate safely with reduced margin from the maximum rated junction temperature or even with no margin at all, unlike silicon-based devices. In any case, operating with reduced FSOA keeps the average chip temperature low enough that significant hot spots do not form, and peak chip temperatures do not cause failures. This is commonly determined experimentally by taking several devices to destruction at various operating conditions, and then applying a safety margin that is statistically significant. Using DCTC analysis, fewer, if any, such destructive tests are necessary, and the true FSOA can be better understood based on the physics of operation.

UnitedSiC JFETs are actually designed for high speed switching and for use in MOSFET-SiC JFET cascodes; hence there is no internal body diode. The efficient design and streamlined manufacturing process that make the UnitedSiC JFET attractive in switch mode power supply (SMPS) applications also make it superior to other device types in high voltage active mode applications.

## 6 Paralleling

The heat dissipation requirement for both SMPS and active mode applications often necessitates paralleling. Both are discussed below as relating to active region characteristics.

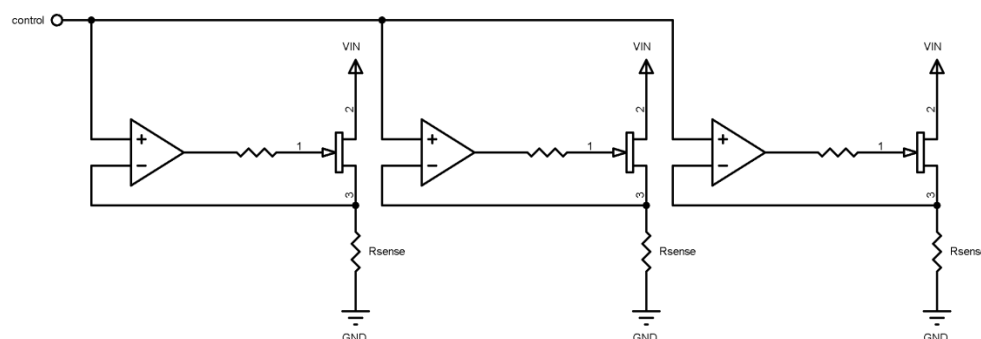
### 6.1 SMPS

Consider a number of parallel devices, with variability between the threshold voltages of each. The device with the lowest threshold voltage begins to turn on first, and to turn off last; thus it has disproportionately higher switching loss and heating. If the overall power loss is high, in other words if operating with a heavy load, then a negative TVTC in the hottest device can cause the dynamic current imbalance to further increase in a self-reinforcing way. This can be a reliability concern in situations where switching loss dominates conduction loss, even if the conduction loss has a positive temperature coefficient, as with MOSFETs and NPT IGBTs for example. This is one reason generous current margin must be applied when paralleling power MOS devices.

With UnitedSiC JFETs, as with power MOS, there is variation in threshold voltage between devices. However, because of reduced TVTC, dynamic current sharing is improved. This is not to say that switching loss is perfectly uniform between devices, but rather that the hottest device is less likely to carry ever-increasing current during switching. This point also applies to UnitedSiC cascodes because the JFET in the cascode handles the high voltage during switching; the cascode MOSFET turns on or off before the JFET completes its switching process. Regarding conduction loss, the positive temperature coefficient of on-resistance ensures thermal equilibrium where no single device goes into thermal runaway due to static current imbalance. As a result, UnitedSiC JFETs and cascodes are highly reliable when paralleled because they are highly stable thermally during both static conduction and during switching.

## 6.2 Active Mode

As with power MOS, part-to-part variation in threshold voltage and temperature-dependent gain is a challenge for steady-state active mode operation of parallel UnitedSiC JFETs. A typical way to solve this challenge is to use individual feedback control of each JFET with an operational amplifier and a current sense resistor [5], as depicted in the simplified schematic in Figure 8.



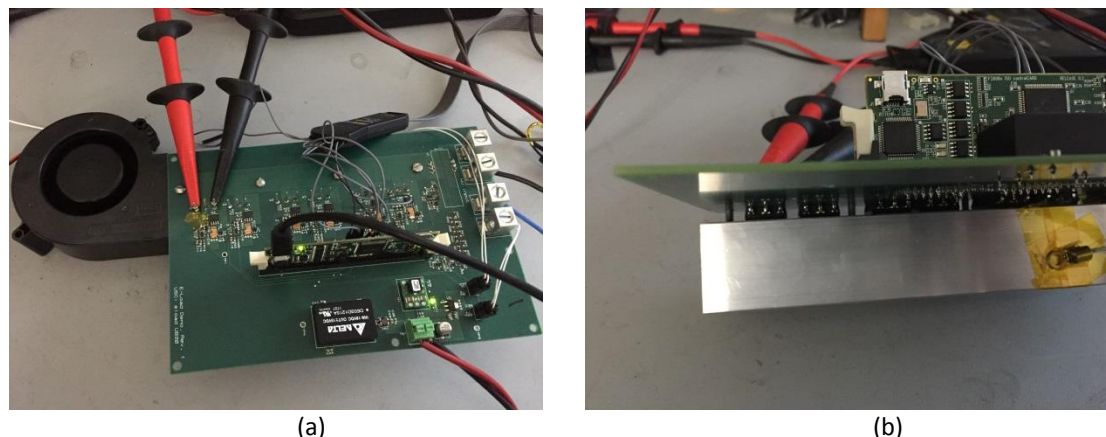
**Figure 8** Simplified example of paralleling UnitedSiC JFETs for steady-state active mode operation

With its negative threshold voltage, each operational amplifier of course requires a negative power supply in order to drive the gate of a UnitedSiC JFET.

## 7 Demonstration

A prototype electronic load board was constructed with six separate channels, each with a UnitedSiC UJ3N120035K3S as the JFET. A top view in Figure 9(a) shows circuitry for the six channels, with each operational amplifier receiving its command signal from a digital control card, and a cooling blower that consumes only about 14 W. In Figure 9(b) the JFETs are visible, “sandwiched” between the circuit board and the heat sink, with no electrically insulating material between the JFET backside drain pad and the heat sink. Each UJ3N120035K3S is always thermally stable for any combination of current and voltage (up to  $BV_{DS}$ ) resulting in 220 W of power dissipation.





**Figure 9** Prototype electronic load test board (a) top view, (b) side view showing JFETs between heat sink and PCB

During preliminary testing, each JFET was loaded to a steady 75 W by adjusting the commanded current as the voltage was increased from 20 to 1000 V, while the peak heat sink temperature reached 97 °C. With better air-cooling, each JFET can handle well over 100 W, and even more with liquid cooling. Testing is still ongoing at the time of writing, but the demonstration of constant load power at elevated heat sink temperature over a wide voltage range validates the theory behind thermal stability of UnitedSiC JFETs with their low TVTC.

## 8 References

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